“Advancements in MM-Wave LNA Design: Optimizing Performance with Modified DS and Post-Linearization Techniques at 26GHz"

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Candidate's Declaration

This is to certify that the work presented in this thesis entitled, , "Advancements in MM-Wave LNA Design: Optimizing Performance with Modified DS and Post-Linearization Techniques at 26GHz", is the outcome of the research carried out byMahin Anjum and Md. Noyon Babu under the supervision of Dr. Apratim Roy, Professor, Department of EEE, Bangladesh University of Engineering and Technology (BUET), Dhaka-1000, Bangladesh.

It is also declared that neither this thesis nor any part thereof has been submitted any- where else for the award of any degree, diploma, or other qualifications.

Signature of Candidates

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Md. Noyon Babu

CERTIFICATION

This thesis titled, **"Advancements in MM-Wave LNA Design: Optimizing Performance with Modified DS and Post-Linearization Techniques at 26GHz"**, submitted Mahin Anjum (1806017) and Md. Noyon babu (1806043), Session: 2021-22, has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Bachelor in Science in Electrical and Electronic Engineering on June,2024

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Abstract

This paper presents a 26 GHzmm wave band low noise amplifier that achieves higher linearity and gain by utilising three alternative linearization methods. In order to achieve high gain and low noise figure, the amplifier is constructed using 0.09um cmos technology and uses a cascode structure as the primary amplifier stage. To improve the third-order interception point (IIP 3), the proposed design makes use of post-linearization techniques and one strong Modified Derivative Superposition Branch. With a noise figure (NF) of 4.51 dB and a simulated gain (S21) of 13.154 dB, this work uses just 20.21mW from a 1.2V power supply. With an input return loss of -8.87dB and an output return loss of -4.04dB, the LNA achieves an IIP3 of -8.25dBm.

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Introduction

1.1 Preamble

Every technological method that doesn't require physical wires or cables is referred to as "wireless" in common usage. The use of wireless technology has boomed significantly nowadays

Benefitted the entire society. It is not difficult to locate. A typical day involves multiple opportunities for wireless communication. Hundreds of millions of people use mobile phones worldwide at the moment. The fact that broadband Internet wireless networks are so widely available not just in offices but also in bustling city center's cafes and public spaces is even more remarkable. Users can now wirelessly transfer data between several linked portable devices, such as laptop computers, mobile phones, and handheld electronic gadgets, with only a single button click. These days, a household may wirelessly connect and operate a large range of appliances, such as laptops, TVs, music systems, window treatments, and lighting. Thanks to the development of intelligent networking, home appliances such as stoves, refrigerators, microwaves, and ovens can now report their contents, statuses, and failures to a central server. The server notifies the user via a screen or text message or gets in touch with the dealer directly for repairs. Furthermore, it is almost impossible to list all the ways that wireless technology is used by people due to the extensive adoption and use of wireless sensor networks for industrial, automotive, and medical applications. In summary, wireless technology has drastically improved human life to the point that it is unimaginable to go back.

Wi-Fi, Bluetooth connections, television broadcasts, cellular networks, and other wireless communication technologies are among the numerous ones that depend on radio frequency radiation. Antennas are necessary for both signal transmission and reception in wireless communication. Electrical signals are used to send and receive electromagnetic (EM) waves, and antennas transform electrical impulses into EM waves. These electromagnetic waves radiate out into space in all directions. This indicates that antennas are present on both the transmitter and the recipient.

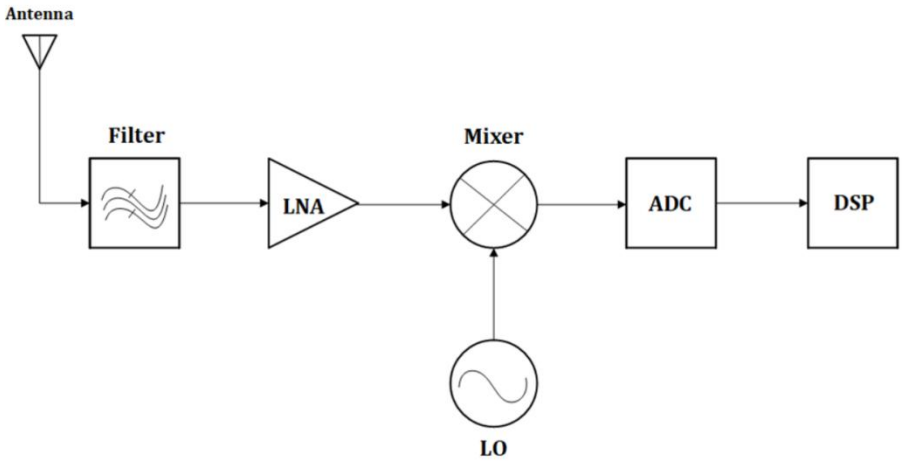

Figure 1.1 :Block diagram of RF receiver

Due to radio waves have to travel such great lengths through the air, these waves are susceptible to atmospheric disturbances and reflection from materials such as metal and buildings.
The resultant high attenuation necessitates the use of signal amplification. Analogue amplifiers may be integrated on a chip more easily thanks to CMOS technology, which enables these amplifiers to be used in a range of situations.Low-Noise Amplifier (LNA) circuits in CMOS technology are implemented as Common Source (CS) or Common Gate (CG) stages.
A designer's expertise and experience play a major role in selecting the right circuit for a particular LNA design. Certain LNA features are more important than others, based on the specific use case.
As seen in Figure 1.1, the Low Noise Amplifier (LNA) is often the first block in a radio receiver. It amplifies the antenna signal to a level appropriate for the first mixer.This means that all other frequencies are effectively attenuated, exposing the LNA to just in-band signals. Only a small portion of the vast range of frequency components produced by the LNA—a non-linear device—are sent along with the input signal. While introducing little noise to the signal during amplification, the optimal LNA will increase the signal-to-noise ratio. This part of an LNA's performance is measured by its noise figure (NF). Because the LNA is adding less noise, a better LNA will have a lower NF. In a cascaded RF system, the input stage often dominates the architecture's NF, but the following stages, which deal with the higher signal amplitudes, tend to dominate the system's IIP3. In the busy wireless environment, the LNA at the beginning of the receiver must, nevertheless, be able to sufficiently suppress the out-of-band interferers. For this reason, an LNA with high linearity and, by extension, high IIP3 is ideal. However, gains in linearity performance may come with unexpected implications, including altered RF settings or decreased gain performance. Thus, there will always be a trade-off between overall linearity and performance increase.

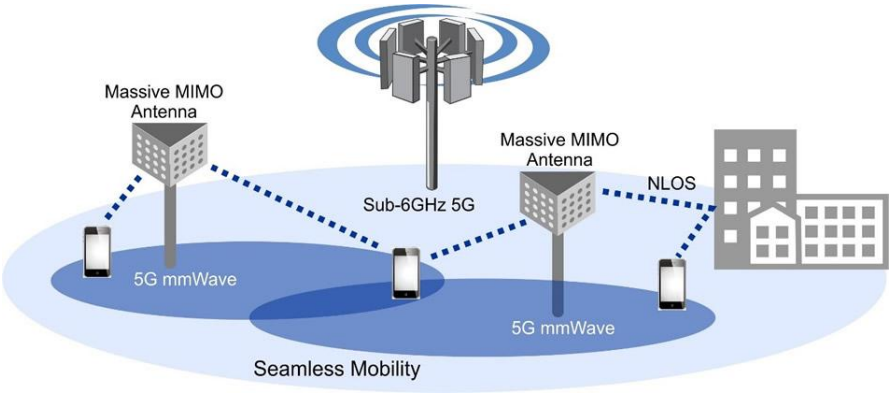

Figure 1.2 : mm wave band 5G technology

Thus, the following is a summary of an LNA's functions:

- Amplify weak signals till they become noticeable.
- Provide a high gain (10–30 dB on average).
- To maintain the signal-to-noise ratio, maintain a low noise figure.
- To enhance power transfer and reduce signal reflections, match the input impedance.
- avoid oscillations or other instabilities, maintain stability.
- Reduce the amount of electricity used, particularly in devices that run on batteries.

1.2 Objectives

The 90nm CMOS technology is used in the design of a low noise amplifier (LNA). Cadence and LTSPICE RF simulation tools are used to model the suggested design.
The objectives of this work are:

- To create the highly linear Low Noise Amplifier (LNA) in the mm wave band that is depicted in figure 1.2 using 90nm CMOS technology for 5G applications.
- Using the derivative superposition, folding cascade, and cascode techniques to increase the LNA's overall gain and linearity
- Maintaining input and output impedance matching in order to sustain high power transmission
- to maintain low power dissipation while obtaining optimum gain and linearity
- to look into how various circuit characteristics affect the LNA's performance.
- To look into and enhance performance metrics such as the LNA's noise figure and scattering parameters

1.3 Thesis Outline

The next six chapters that comprise this thesis begin with this introduction. These are the following:

Chapter 1:

The first chapter introduces the thesis. The purpose of this work is explained in this chapter. A overview of the literature on low noise amplifiers in radio frequency communication is offered to help you better understand the motivation for this study. A brief overview of the expected outcomes is also included in the thesis. We also demonstrate the progress we've made in the field of analogue radio frequency circuits with this thesis.

Chapter 2:

The performance figures of merit of the amplifier are shown as design parameters in Chapter 2. The constraints and challenges of the design are explained, and trade-offs between important parameters and how they affect system performance are illustrated. Here is also where the power consumption and stability requirements of the amplifier are covered.

Chapter 3:

In Chapter 3, linearization techniques for CMOS LNAs are covered. Circuit-level analysis has also been done on these amplifiers. The techniques for removing distortion and noise are also covered in this chapter.

Chapter 4:

Chapter 4 discusses the suggested architecture and the front-end amplifier design with post-distortion branches as well as super-position techniques. Included are the output matching, input matching, and linearity performance of the amplifier.

Chapter 5:

The proposed amplifier is discussed, and the simulated results are presented in Chapter 5. This chapter also includes a comparison of the LNA’s performance to that of other previously reported LNAs.

Chapter 6:

In Chapter 6, a summary and various possibilities for further research are briefly covered.

Chapter 2

Literature Review

Low Noise Amplifiers (LNAs) are essential components in modern communication systems, responsible for amplifying weak signals while minimizing additional noise, thereby ensuring signal integrity. With the rapid advancements in wireless technology, particularly in 5G applications, the demand for high-performance LNAs has surged. Recent research focuses on optimizing key performance metrics such as noise figure, gain, linearity, and power consumption through innovative design techniques and advanced fabrication processes. This literature review examines the latest developments in LNA design, highlighting various approaches and their impact on performance. By understanding these advancements, we can better address the challenges in creating efficient and robust LNAs for next-generation communication systems.

According to [1] , The paper details a high-performance low-noise amplifier (LNA) using 22-nm SOI-CMOS technology, achieving a minimum noise figure (NF) of 1.7 dB at 28 GHz, and maintaining an NF below 1.98±0.25 dB across a 10-GHz range. With a peak gain of 21.5 dB at 22 GHz and a wide bandwidth of 19-36 GHz, it offers excellent signal amplification and frequency versatility. Input and output return losses better than 10 dB ensure effective impedance matching. The LNA also features adjustable power consumption, maintaining performance with minimal degradation when power is reduced. In a comprehensive review by[2], it represents a 24-44 GHz low-noise amplifier (LNA) designed using 45nm CMOS SOI technology, aimed at covering all major 5G frequency bands. The UWB LNA achieves a maximum gain of 20 dB and maintains a noise figure (NF) between 4.2 and 5.5 dB across its bandwidth. Compared to a narrowband 28 GHz LNA, the UWB LNA exhibits a slight NF increase of 0.5 dB and consumes 40 mW more power. However, its broad frequency coverage supports multi-band 5G operations, eliminating the need for multiple multiplexed LNAs, and serves as an effective amplifier for broadband sliding-IF down conversion receivers in Ka-band phased-array systems.
The work of [3] introduces a high-gain low-noise amplifier (LNA) designed using 0.25 µm SiGe:C BiCMOS technology, achieving notable performance metrics. The key innovation is the use of a 3-winding transformer-based dual-tank matching technique, which facilitates wideband simultaneous noise and power matching within a compact size. The LNA delivers a peak gain of 28.5 dB at 32 GHz with a 3-dB bandwidth ranging from 29 to 37 GHz, ensuring low noise figures between 3.1 to 4.1 dB and effective power matching. Additionally, it demonstrates robustness and efficiency in practical applications, evidenced by its measured input IP3 and P1dB at 32 GHz, alongside a total DC power consumption of 80 mW. This work exemplifies a balanced approach to optimizing gain, noise figure, bandwidth, and chip size for multi-functional front-end systems.[4] literature on dual-path noise-canceling LNAs focuses on enhancing performance by mitigating noise in both signal paths simultaneously. Utilizing a combination of common gate (CG) and common-source (CS) amplifiers, along with amplitude-adjusting stages

and a three-stage transformer, the LNA achieves low noise figures and wide band operation from 22.9 to 38.2 GHz. Implemented in 28-nm CMOS technology, it demonstrates a low power consumption of 18.9 mW at 0.9 V, with a peak gain of 14.5 dB. This design addresses challenges in noise reduction and inter stage matching crucial for applications like high-frequency wireless systems such as 5G.

The work on [5] on the 28 GHz low-noise amplifier (LNA) in 90 nm SOI CMOS technology highlights its suitability for 5G applications, focusing on low power consumption and stability considerations. The design incorporates a 1200 Ω bias resistor to ensure unconditional stability across the operating band, achieving a maximum gain of 18.1 dB and average noise figure (NF) of 3.1 dB. Key features include gate bias points set at 0.55 V for low power and temperature stability, with measured S11 below −10 dB and S12 below −25 dB over the operating frequency range. With a compact core area of 0.16 mm², the LNA exhibits minimal gain and NF variations across temperature ranges, demonstrating its potential for reliable performance in high-frequency wireless systems like 5G.This work of [6] introduces a two-stage cascoded CMOS LNA tailored for 28 GHz 5G applications, featuring a novel power-saving technique through common drain envelope detection. Dual inductive peaking and stagger tuning techniques extend the bandwidth to 2.25 GHz (26.75-29 GHz) with a gain of 22 dB. Inductive source degeneration reduces the Noise Figure (NF) to 2.3 dB in the first stage. The envelope detector, employing a common drain transistor with active components, enables efficient power management, achieving a 25.26% reduction in power consumption during sleep mode. The LNA operates at 9.5 mW (active) and 7.1 mW (sleep) from a 1.5 V supply, occupying 0.1235 mm² in 90 nm technology. Robustness across process corners and temperatures is validated through Monte-Carlo analysis, confirming its suitability for demanding 5G communication systems.In [8] paper, a 3-stage balun-less differential-ended LNA is introduced, leveraging a cascode topology with CMOS push-pull technique to enhance performance parameters such as linearity, reverse isolation, and noise figure. The design achieves a gain of 25.5 dB, NF of 1.46 dB, input reflection coefficient of -15.8 dB, and IIP3 of -11.6 dBm, resulting in an impressive Figure of Merit (FOM) value of 78.29 with unconditional stability. This makes the proposed LNA a promising choice for mm-wave applications requiring robust performance metrics.

The work of [9] introduces a low power CMOS LNA design in TSMC 0.18 μm RF CMOS technology. The LNA features a current-reused structure to minimize power consumption by simultaneously operating two transistors with the same DC current. Stagger-tuning techniques are employed to achieve gain flatness across the 3.1 to 10.6 GHz bandwidth, with resonance points strategically set at 3 GHz and 10 GHz. Noise canceling is implemented to mitigate noise generated by the first transistor, resulting in a flat gain (S21) of 14 dB with excellent input impedance matching (< -10 dB) and a minimum noise figure of 2.9 dB. The LNA operates at 15.2 mW from a 1.8 V supply, demonstrating its suitability for UWB applications.[10] paper introduces a highly linear CMOS LNA. The design enhances input second- and third-order intercept points (IIP2 and IIP3) by eliminating common-mode inter modulation components through a unique structure involving cascaded differential pairs with cross-connected outputs. This approach effectively cancels out common-mode currents, improving linearity. Additionally, the LNA optimizes noise performance by canceling thermal noise from input and auxiliary transistors. Post-layout simulations in a 90 nm RF CMOS process demonstrate a power gain of 9.5 dB, bandwidth of 8 GHz (2.4 GHz to 10.4 GHz), and mean IIP3 and IIP2 values of +13.1

dBm and +42.8 dBm, respectively. The LNA exhibits S11 below -11 dB across the frequency range and operates at 14.8 mW from a single 1.2 V supply.
This paper [11] presents a 0.5-V low noise amplifier (LNA) designed for a 2.4 GHz medical application using a 0.18 μm CMOS process. The LNA employs a novel modified complementary current-reused architecture, integrating forward body bias technology to enhance noise performance and minimize body leakage. A diode-connected MOSFET forward bias technique is utilized for this purpose. Additionally, a notch filter isolator with harmonic rejection is implemented to improve linearity at low voltage. Experimental results demonstrate the LNA achieves 18.7 dB power gain and 1.52 dB noise figure, while consuming only 4.2 mA of DC current at 0.5 V supply voltage.The paper [13] details a low noise amplifier (LNA) design for 5G applications using 180nm CMOS technology, specifically targeting operation at 26 GHz. The LNA architecture comprises a two-stage configuration: a common-source stage utilizing noise cancellation techniques to minimize noise figure (NF), followed by a Cascode stage to enhance power gain and improve reverse isolation. Simulations conducted in Advanced Design System (ADS) software show the LNA achieves a gain of 17.105 dB and NF of 1.016 dB at 26 GHz. Impedance matching ensures S11 of -19.185 dB and S22 of -38.884 dB, validating its suitability for high-frequency applications in wireless communication systems.

The work of [15] study presents a low-noise feedback amplifier (LNA) designed in 22-nm fully depleted silicon-on-insulator (SOI)-CMOS technology. Operating at 28 GHz, the LNA achieves a minimum noise figure (NF) of 1.7 dB, with NF maintained below 1.98±0.25 dB over a 10-GHz range. The two-stage LNA exhibits a peak gain of 21.5 dB at 22 GHz and a bandwidth (BW) for |S21| spanning 19–36 GHz. Input and output return losses are superior to 10 dB across an effective BW of 22–32 GHz. The third-order input intercept is -13.4 dBm at peak gain, with a power dissipation of 17.3 mW. The LNA incorporates continuous dc power control via FET backgate modulation, reducing power consumption by 5.6 mW with minimal impact: NF increases by less than 0.5 dB, peak gain decreases by 3.6 dB, and input return loss remains unchanged within the effective BW.

[18] presents a CMOS variable gain LNA designed for 28-GHz 5G integrated phased-array transceivers, focusing on maintaining high third-order intercept point (OIP3) across all gain settings. The LNA features three stages with digitally controlled gain optimized to achieve higher OIP3 at lower gain levels. Double-tuned transformers couple the stages for maximum group delay flatness. Fabricated in a 40-nm CMOS process, it offers 18–26 dB gain with 1-dB gain steps, OIP3 ranging from 12 to 14.5 dBm, and a noise figure between 3.3–4.3 dB across the 26–33 GHz frequency range. Power consumption varies from 21.5 to 31.4 mW, with a root-mean-square error of gain steps less than 0.38 dB, demonstrating high linearity and efficiency suitable for advanced millimeter-wave communication systems.

Chapter 3:

Design Parameters

Low noise amplifiers play a crucial role in radio receiver performance (LNAs). A receiver's sensitivity to signals, its ability to filter out undesired ones, and its vulnerability to receiving errors are some of the factors that can be used to determine the quality of its design. Enhancing the receiver's front end's efficiency is the responsibility of an RF engineer, with a focus on the starting active element. All receivers require a sensitive enough LNA to separate the remaining signal from interference and background noise in order to reliably retrieve the included information. The LNA's noise figure, gain, bandwidth, linearity, and dynamic range—all of which the designer can adjust—all have an immediate impact on the sensitivity of the receiver. Nonetheless, to get optimal performance with the lowest changes in the amplifier's other attributes, mastery of the active device, impedance matching, and fabrication and assembly details is required.

3.1 Noise

In radio communication systems, undesired signals that reduce the system's sensitivity are referred to as noise. Additional noise and interference are picked up by the signal as it travels through a medium, and these must be eliminated at the receiving end. But the LNA adds its own noise to the received signal because it is an active component of the receiver. Since the amplifier is the receiver's first block, it contributes significantly to the overall noise.

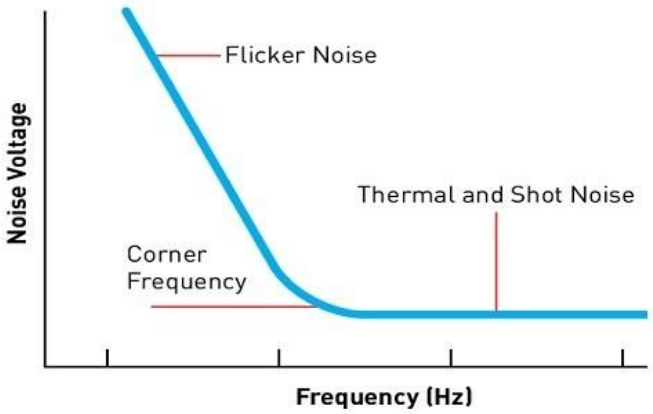

Figure 3.1: Flicker and thermal noise contribution vs frequency.

3.1.1 Noise classification

Several noise generators are available that generate noise from different sources. Typical forms of background noise include:

- Shot noise
- Flicker noise
- Thermal noise

Shot noise

Shot noise, also known as Schottky noise or Poisson noise, is a random fluctuation in electric current or signal caused by the discrete nature of electric charge carriers. It follows a Poisson distribution and is directly proportional to the square root of the average current passing through a device. Mathematically, the standard deviation (σ) of shot noise current (I_shot) can be expressed as:

$$\sigma = \sqrt{2qI\Delta f}$$

where:

- q is the charge of an electron,
- I is the average current,
- Δf is the bandwidth of the signal or the frequency range over which shot noise is measured.

Shot noise is significant in electronic devices operating at low currents, such as photodetectors and semiconductor devices, and it can limit the accuracy of measurements and the sensitivity of devices. Despite being considered a source of noise, shot noise is also utilized in applications such as shot noise thermometry and shot noise spectroscopy.

Flicker Noise

Due to a physical process, the flicker noise in MOSFETs is unpredictable and is related to the interface between the silicon substrate (Si) and gate oxide (SiO2). At the Si and SiO2 and contact, carriers are trapped and released, resulting in a fluctuation in the channel that sounds like flicker noise. Flicker noise scales as 1/f, therefore at higher frequencies it is mainly ignored. This phenomena is represented by a voltage source that produces flicker noise and is coupled in series with the gate. The flicker noise can be expressed as:

$$K_f = \sqrt{\frac{k_f}{CoxWL_f}}$$

Cox, W, and L are the gate oxide capacitance per unit area, width, and length of the MOSFET, respectively; k_f is a constant that varies depending on the manufacturing process. Because the kf

for p-channel devices is lower than that of n-channel devices, PMOS transistors show less flicker noise.

Thermal Noise

Electrons move randomly in circuits, which causes thermal noise. The power of a thermal noise signal is expressed as:

$$P_n = 4k_BTF$$

where T is the system's temperature in Kelvin, f is its band-width in Hz, and k is the Boltzmann's constant. The resistor's thermal noise voltage model is as follows:

$$v_n = \sqrt{4k_BRTF}$$

Where, R is resistance value in ohm.
Because of the carrier movement in the channel, MOSFETs also show thermal noise. As seen in Fig. 3.2, this noise is modelled by placing a current source in a parallel MOSFET with a conducting channel. When the device operates in triode mode, this noise current is modelled as

$$I_n = \sqrt{4k_BTg_{d_0}f}$$

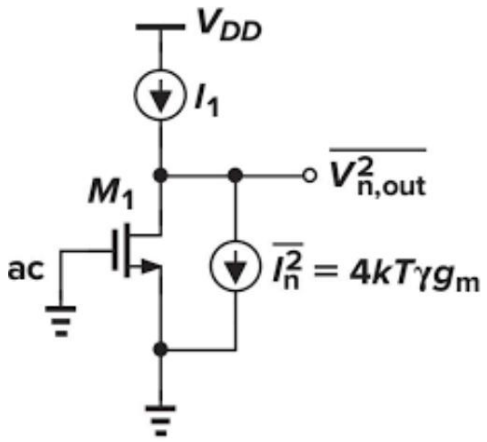

Figure 3.2: MOSFET channel thermal noise representation.

3.1.2 Noise Performance

Several factors can be used to determine the level of noise in an electrical signal. Suchas

Noise Figure

The noise factor of a device shows how much the signal-to-noise ratio has declined. The input signal intensity and the output signal strength, as depicted in figure 3.3, are compared by the

SNR. The Noise Factor will never be more than 1 because it is guaranteed that the output signal-to-noise ratio will be lower than the input signal-to-noise ratio. Noise reduction improves device performance. One way to explain the noise factor is:

$$F = \frac{\frac{S_i}{N_i}}{\frac{S_0}{N_0}}$$

Where

S_i = Signal level at input

N_i = Noise level at input

S_o = Signal level at output

N_o = Signal level at output

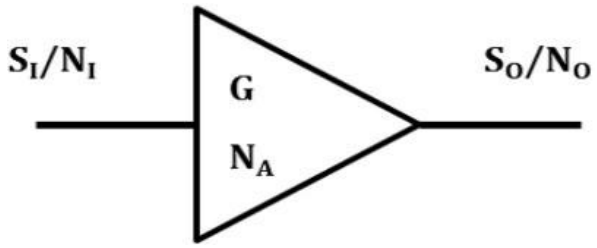

Figure 3.3: Noise factor representation.

Noise Figure

The noise figure is a metric used to measure the noise performance of an amplifier or radio receiver. The noise figure decreases with increasing performance. The contribution of a certain component to the system's overall noise level is described by the noise figure. It might be a mixer, a preamp, or even the complete receiver. The noise figure can be more useful than the signal-to-noise ratio in determining a receiver's efficacy. which is able to be stated as:

$$\text{Noise Figure} = 10\log_{10}\left(1+\frac{Sout}{\text{Sin}}\right)$$

An input signal-to-noise ratio of 4:1 and an output signal-to-noise ratio of 3:1 would yield a noise factor of 4/3 and a noise figure of 10 log (4/3) or 1.25 dB, respectively. Because logarithms

are used to split numbers, if the signal-to-noise ratios are provided in dB, the noise level can be found by subtracting the two figures. To put it another way, if the signal-to-noise ratio was 13 dB at the input but only 11 dB at the output, the circuit's noise figure would be 13 - 11 or 2 dB.
A multistage amplifier receiver's overall noise figure can be expressed as follows:

$$\text{Overall Noise Figure} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}$$

Because it may describe the noise performance of different components of a system with a single number, the noise figure is a valuable parameter. One can evaluate the overall performance of the system by knowing the gain settings and each component's noise figure. The system's noise figure can then be easily calculated and optimized.

3.2 Scattering Parameters

A mathematical tool for determining the distribution of radio frequency (RF) energy in a network with several exits is the scattering matrix. The S- matrix allows for the accurate description of incredibly complex networks as simple "black boxes." An RF signal that is incident on a port will do one of three things: it will either enter the incident port and exit there, or it will enter the port and exit at (or scatter to) some or all of the other ports (perhaps amplified or attenuated).

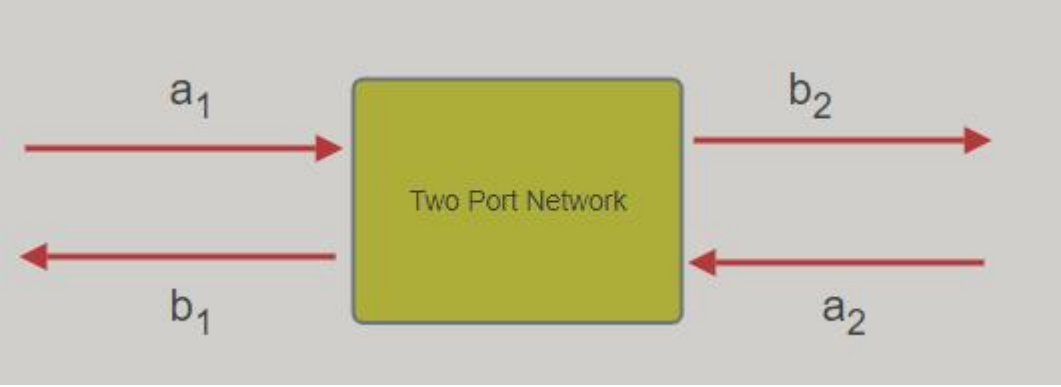

Figure 3.4: Two port network.

The Dual Port The majority of the energy that is incident is lost as heat or maybe as electromagnetic radiation. The S-matrix for an N-port has N2 coefficients (S-parameters), each of which represents a distinct input-output combination. S-parameters are complex numbers made up of real and imaginary, or magnitude and phase, components since the network alters the incident signal's both amplitude and phase. Since signal strength is the metric that receives the most attention, it is sometimes the only one that is discussed. What difference does it make if the signal's phase is changed by an amplifier or attenuator? You care primarily about your financial gain (or loss). The S-parameters for any non-ideal network deviate from the values given for a

particular frequency and system impedance as a function of frequency. A matrix representing S-parameters should have the same number of rows and columns as ports. The stimulated port, or input port, is indicated by the j subscript in the S-parameter Sij, and the receiving port is indicated by the i subscript. As a result, S11 is the ratio of the amplitude of the incident signal at port 1 to that of the reflected signal. Transmission coefficients are S-parameters that describe events at one port when aroused by a signal incident at another, whereas reflection coefficients are S-parameters that only describe events at a single port and sit along the diagonal of the S-matrix. The following are the S matrices for a network with 1, 2, and 3 ports:

$$\begin{bmatrix} b_1 \end{bmatrix} = \begin{bmatrix} S_{11} \end{bmatrix} \begin{bmatrix} a_1 \end{bmatrix}$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

The network with two ports (figure 3.4) The foundation for building higher-order matrices for more intricate networks is the S-parameter matrix. The S-parameter matrix is related to the incident power waves that are reflected in this example by the formula:

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

The 2-port S-parameters have the following typical descriptions:

- S11 is the input port voltage reflection coefficient
- S12 is the reverse voltage gain
- S21 is the forward voltage gain
- S22 is the output port voltage reflection coefficient

In Low Noise Amplifiers, power gain should be maximised without adversely affecting signal quality. Alternatively, if we express S21 in terms of scattering characteristics, we want it to be as high as possible inside our target band. There will be some signal loss in an operational amplifier at both the input and output. Not just amplifiers, but any two-port network (such an antenna and

a receiver) can benefit from this. Our goal is to minimise S11 and S22 losses while staying within our target range. Additionally, reverse isolation is an essential component of a two-port network. For example, it is not desired for an alteration in the output signal to impact the input signal. Reducing S12 in the intended frequency range is therefore also crucial.

3.3 Input Matching

The first step in the amplifier chain of the receiver is the low-noise amplifier (LNA). For the best possible power transfer between the two, as seen in figure 3.5, the input impedance of the LNA and the output impedance of the antenna must match. Noise is caused by signal reflection and mismatched impedance. Since input impedance matching affects power transmission efficiency, it is an important design parameter for LNAs. The S11 parameter of a two-port network indicates the ratio of the reflected signal power to the input signal power at port 1. Decibels (dB) are used to indicate S11, with values less than -10dB being preferable. 10% of the input power is reflected when the S11 value is -10 dB. In the same way, the output impedance of the LNA needs to match the input of the stage after it. Using S22 of the S parameter, output impedance matching is evaluated. To increase the strength of weakly received signals, another design performance criterion that needs to be enhanced is power gain (S21). In order to optimize the power transfer from the amplified output of the LNA to the conjugate planes, the next stage's input impedance is required.

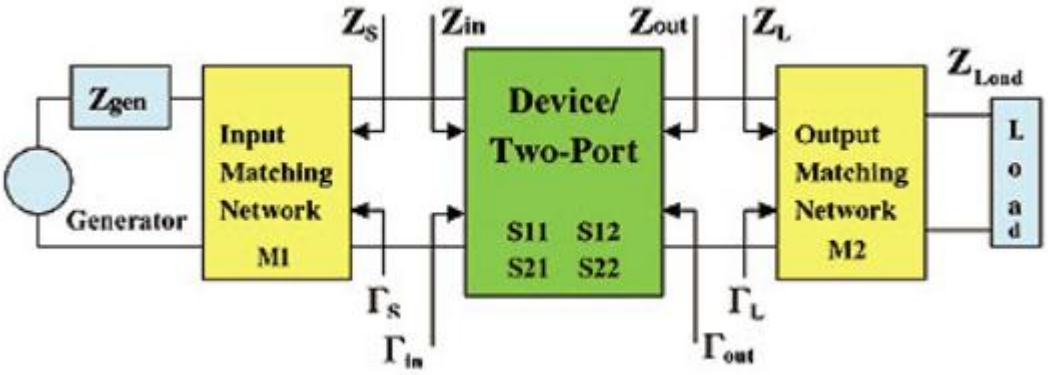

Figure 3.5: Two port network impedance matching.

For example, the impedance measurement from left to right in the plane in Figure 3.5 must be Zin*. It is possible to make a lossy matching network totally reactive by changing its bounds, adding all losses to R0 or Zin. Consequently, the property of conjugate impedance remains relevant.

Low-noise amplifiers (LNA) typically determine the sensitivity and noise figure of receivers and other high-frequency devices. While a wide variety of efficient low-noise transistors based on various process technologies are already on the market, obtaining superior amplifier low-noise performance depends critically on the input impedances of the LNA devices and the impedance-

matching topologies chosen. The ideal topology for a given impedance of the device can be found by taking these options into account.

3.4 Linearity

A low noise amplifier's different performance features include gain, frequency bandwidth, power output, linearity, efficiency, noise, and input/output matching. In contrast, wireless applications require linearity. More linearity is required for broadband modulation techniques like wideband code division multiple access (WCDMA), high speed packet access (HSPA), and orthogonal frequency division multiplexing (OFDM). When describing Low Noise Amplifiers, the following linearity parameters are most frequently used:

- 1dB compression point
- Third order intercept point

Greater values for these variables are ideal. It suggests that the output power will stay linear for far larger ranges of input power.

3.4.1 1db Compression Point

An input-output relationship for a memory-less system can be written as:

$$y(t) = a_o + a_1x(t) + a_2x(t)^2 + a_3x(t)^3 + ...$$

if

$$x(t) = Acos(wt)$$

Then,

$$y(t) = a_o + a_1Acos(wt) + a_2A^2cos(wt)^2 + a_3A^3cos(wt)^3 + ...$$

$$y(t) = a_1Acos(wt) + \frac{a_2A^2}{2}(1 + cos(2wt)) + \frac{a_3A^3}{4}(3cos(wt) + cos(3wt))$$

$$y(t) = \frac{a_2A^2}{2} + (a_1A + \frac{a_3A^3}{4})cos(wt) + \frac{a_2A^2}{2}(cos(2wt)) + \frac{a_3A^3}{4}(cos(3wt))$$

The gain that A experiences cos(wt) fluctuates considerably as A gets larger since it is equal to $(a_1 + 3a_3A^2)/4$. If A1 and A3 are less than 0, then the gain decreases as A increases. The 1dB Gain Compression point, which is defined as the signal's input power level at which the gain deviates by 1dB from its interpolated extended value as illustrated in Figure 3.6, can be used to quantify this effect. The output power decreases by 1dB from its ideal value when plotted on a logarithmic scale as a function of input power at a 1dB compression point. By equating compressed gain to one decibel below optimum gain, one can determine the 1 dB compression point.

$$20\log(a_1 + \frac{3a_3A^3}{4}) = 20log(a_1) - 1dB$$

Gain A at this point is called A_{in1dB}

$$A_{in1bd} = \sqrt{.145\frac{|a_1|}{|a_2|}}$$

A 1 dB compression, which translates to a 10% gain reduction, is frequently employed to characterise radio frequency systems.

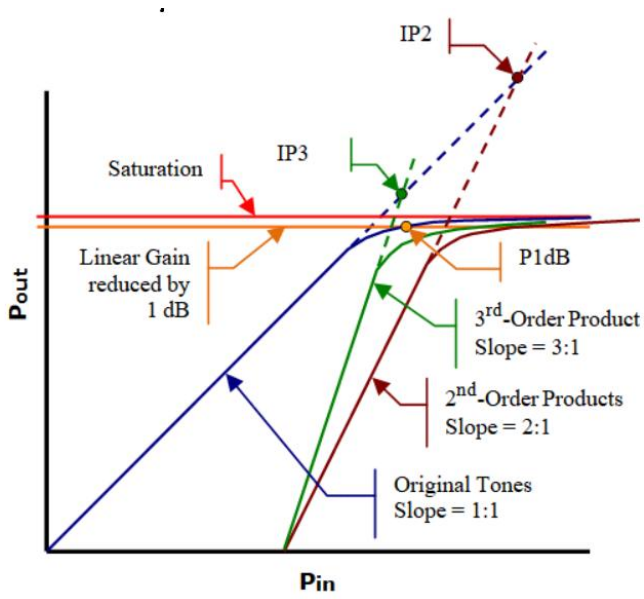

Figure 3.6: IIP3 and 1dB compression point.

3.4.2 Third Order intercept Point

An amplification circuit that deviates from linearity will produce output frequencies that are harmonics of the input frequencies; if the amplifier's second, third, or higher harmonics are causing issues, they can usually be easily filtered out. However, non-linearity can result in a mixing effect between multiple signals; if the signals are close in frequency, some of the sum and difference frequencies created by the intermodulation products can occur within the amplifier's bandwidth. These will begin to interfere with the signals you are attempting to amplify because they cannot be removed. Therefore, it is essential to optimise the biassing, signal levels, and other parameters to maximise linearity and minimise intermodulation distortion (IMD) products.Two signals, f1 and f2, that occur inside the amplifier bandwidth are depicted in Fig. 3.7. New signals f1 - f2 and f1 + f2 are generated with distortion. Most of the time, they are

filterable. These signals, however, will also combine with the higher, second, and third harmonics to create a variety of signals that could interfere with the amplifier pass band.The third-order products, 2f1-f2 and 2f2-f1, are the most problematic. The output power and input power connection resembles the curve that shows the 1 dB compression (Figure 3.6). The signal at the first order is plotted here. Observe how the gain curve has flattened due to compression.

This graph also displays the third-order product's signal levels. On a logarithmic scale, the mathematics of mixing predicts that the gain rate for third-order products will be three times faster than that of first-order products. The linear parts of the two gain curves overlap when the third-order signals have the same amplitude as the first-order or input signals, as seen in Figure 3.6.

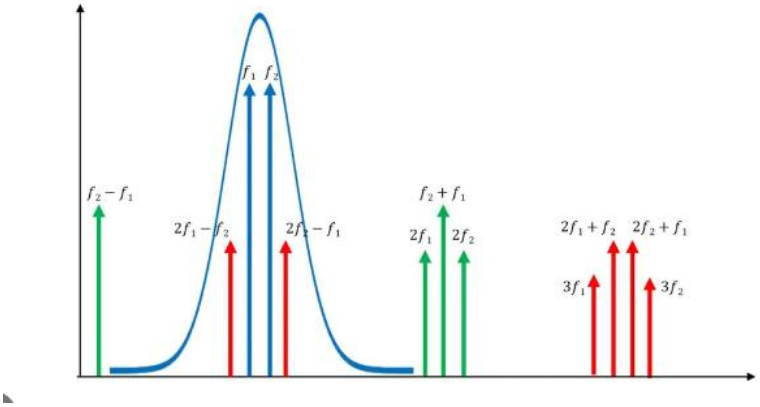

Figure 3.7: Third order frequency spectrum.

The IP3 value can be obtained from either the input or the output; from the output axis, this number is represented as OIP3. The value IIP3 is read from the input axis; the stronger the linearity and the smaller the IMD, the higher the output at the intercept needs to be. This is the intercept at the third-order level; in principle, it exists, but in practice, it is impossible to attain. Nevertheless, it helps in testing the amplifier's linearity.

3.5 Power Consumption

Designing for battery-operated devices requires careful consideration of how much power is used. Because of the low power dissipation architecture, the cost of the cooling system may be decreased and more functionality can be added to the chip without affecting battery life. The following formula can be used to estimate a Low-Noise Amplifier's (LNA) power consumption:

$$P=V_{dd}I_{dd}$$

where Vdd is the supply voltage in volts, Idd is the quiescent current in amperes, and P is the power usage in watts. The DC current that passes through the LNA in a steady state while it is not amplifying any signal is known as the quiescent current, or Idd. Usually, the LNA datasheet has specifications for this current.

Other elements that can impact an LNA's power consumption include the load impedance, gain setting, and input signal level. On the other hand, depending on the supply voltage and quiescent current, the aforementioned calculation offers a ballpark approximation of the power usage.

3.6 Stability

LNA stability places limits on its gain. It is quite significant if we discover that the source/load impedance of circuits in a wireless device is changeable. It is necessary for an LNA to be unconditionally stable over the whole range of feasible values for both the source and the load impedance, since a change in either one could result in instability. Furthermore, even if the LNA becomes unstable and oscillates at a frequency different from its operating frequency, excessive signal oscillation may still compress the gain of the LNA and impair its performance, therefore stability at all frequencies needs to be ensured. Two prerequisites must be met in order for stability:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|^2\,|S_{21}|^2} > 1$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1$$

where Sij denotes the LNA's scattering parameters. Since the output of the LNA in a current RFIC design is not matched to 50 and is connected to the mixer's input without the use of a power matching network, S22 approaches 1 if the LNA has a good enough degree of reverse isolation, with S12 approaching zero.

$$K = \frac{1 - |S_{22}|^2}{2\,|S_{12}|^2\,|S_{21}|^2} > 1$$

For S11 less than 1, the upper limit of S21 becomes,

$$|S_{21}| < \frac{1 - |S_{22}|^2}{2\,|S_{12}|^2}$$

A 100 dB difference between the highest and lowest recorded signal levels is typical in mobile phone networks. As a result, the user's distance from the base station should determine how much gain the system uses for the receive path. Implementing gain variation or gain switching in the receive channel requires the LNA.

For example, it is not unusual for cellular mobile phone networks to have a fluctuation of 100 dB between the highest and lowest reported signal levels. As a result, the user's distance from the base station should determine how much gain the system uses for its receive path. An essential part of achieving gain variation or gain switching in the receive channel is the LNA.

Chapter 4

Architectures

The power series' first three components represent approximations for an input-X and output-Y weakly nonlinear amplifier.

$$Y = g_1X + g_2X^2 + g_3X^3$$

where g_1, g_2, and g_3 represent the amplifier's linear gain and second- and third-order nonlinearity coefficients, respectively. Making g_2,g_3 as minimal as possible is the aim of linearization; only the linear term g1 is retained, so $Y = g_1X$. LNA nonlinearity is mostly caused by two factors:

- The impact of nonlinear transconductance that is "input limited," which converts a linear input voltage into a nonlinear drain current.
- The device is said to as "output limited" when the drain source voltage VDS is low, meaning it is functioning in the near linear area. This is when the effect of the nonlinear output conductance g_{DS} is obvious.

4.1 Feedback

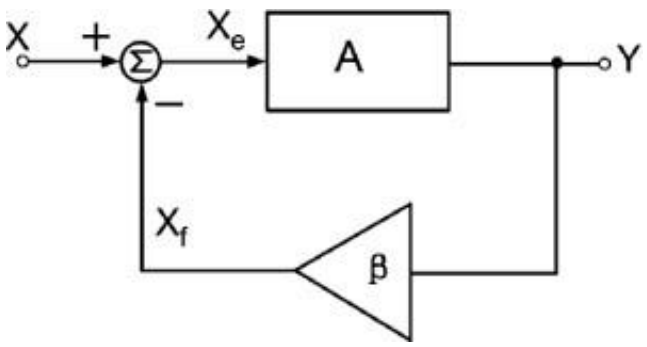

Figure 4.1: Nonlinear amplifier with negative feedback

The negative feedback technique is shown in Fig. 4.1 using a nonlinear amplifier A and a linear feedback factor B, where X and Y are the input and output signals, respectively. X_f represents the feedback signal, while X_e minus X_f represents the output signal. We obtain the third-order closed-loop power series for Y if the nonlinear amplifier A is well-modeled by the preceding equation.

$$Y = b_1X + b_2X^2 + b_3X^3$$

$$b_1 = \frac{g_1}{1 + t_0}$$

$$b_2 = \frac{g_2}{(1 + t_0)^3}$$

$$b_3 = \frac{1}{(1 + T_0)^4}(g_3 - \frac{2g_2^2 T_0}{g1(1 + T_0)})$$

where $T_0 = g_1B$ is the linear open-loop gain and $_{b1,2,3}$are the closed-loop linear gain and second/third order nonlinearity coefficients, respectively. The closed loop system's and amplifier A's IIP2 and IIP3 are

$$A_{IIP2,amplifier} = \sqrt{\frac{g_1}{g_2}}$$

$$A_{IIP2,closeloop} = \sqrt{\frac{b_1}{b_2}} = \sqrt{\frac{g_1}{g_2}(1 + T_0)^2}$$

$$A_{IIP3,amplifier} = \sqrt{\frac{4g_1}{3g_3}}$$

$$A_{IIP2,closeloop} = \sqrt{\frac{4b_1}{3b_3}} = \sqrt{\frac{4g_1(1 + T_0)^3}{3g_3(1 - \frac{2g_2^2 T_0}{g_1 g_3(1+T_0)})}}$$

Therefore, when g2 = 0, negative feedback increases AIIP2 by a factor of (1 + T0) and increases AIIP3 by a factor of (1 + T0) 3/2. For common MOSFET biases, where g1 and g3 have opposite signs, as seen by (4.8), nonzero g2 degrades IIP3. We refer to this phenomena as "second-order interaction." Stated differently, there are two causes of third-order nonlinearity while the amplifier is in feedback:

- Third-order nonlinearity in an intrinsic amplifier.
- "Second-order interaction" (resulting from feedback and the amplifier's intrinsic second-order nonlinearity).

Nevertheless, compared to baseband circuits, feedback linearity enhancement is less successful for LNAs due to:

- The strict LNA gain, noise, and power requirements prevent a large open loop gain T0.
- The second-order nonlinearity indirectly contributes to the IM3 through "second-order interaction."

4.2 Optimal Biasing

i_d can be expressed as :

$$i_d = g_1(V_{in} - V_s) + g_2(V_{in} - V_s)^2 + g_3(V_{in} - V_s)^3$$

Assume that transconductance non-linearity, as represented by the preceding equation, is the primary cause of a MOS transistor's nonlinearity. The sign of g3 is inverted, whereas g2 is always positive.

- Small Vgs: $g_3 > 0$ due to the transistor's weak inversion operation, where the exponential requirement is met by the I_{ds} vs v_{gs} relationship.
- Large Vgs: $g_3 < 0$ due to gain compression caused by velocity saturation and mobility decline. Optimal biassing involves biassing the transistor at its "sweet spot," $g_3 = 0$.

The following are the limits of the optimal biassing technique, despite its apparent simplicity.

- We suggest constant-current or constant-gm biassing instead of constant-voltage biassing because process disturbances, such Vth, can affect the cancellation.
- Owing to the method's dependence on operating points, distortion cancellation can only be accomplished over a relatively narrow input-signal amplitude range.

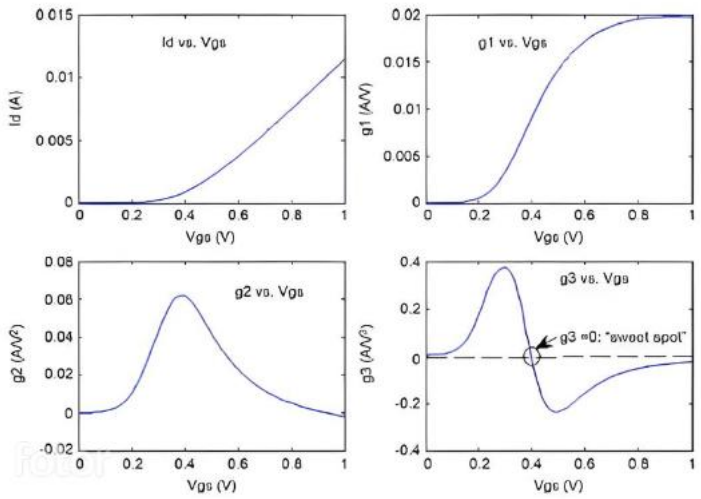

Figure 4.2: The results of an optimal biasing example

- Only a comparatively small range of input-signal amplitudes may achieve distortion cancellation due to the method's dependence on the operating point.
- The "second-order interaction" increases with source degeneration inductance, which results in a progressive fading and disappearance of the IIP3 peak in the "sweet spot."
- The sweet spot and IIP3 peak decrease more frequently due to parasitic effects.
- Biassing the transistor to $g_3 = 0$ restricts transconductance in the input stage by increasing noise figure and decreasing gain.

In summary, the highest potential third-order intrinsic transconductance nonlinearity is represented by the "sweet spot," which is a single transistor's feature. There will be several other problems that will compromise the "sweet spot" improvement in IIP3. Furthermore, others contend that there isn't a "sweet spot" in real LNAs because of input/output networks and parasitics.

4.3 Feedforward

Equation (4.10) indicates that more degrees of freedom are required for the simultaneous cancellation of and with little effect on g1. One way to accomplish this simultaneous cancellation is to create more nonlinear voltages and currents, then sum (or sub-tract) them.

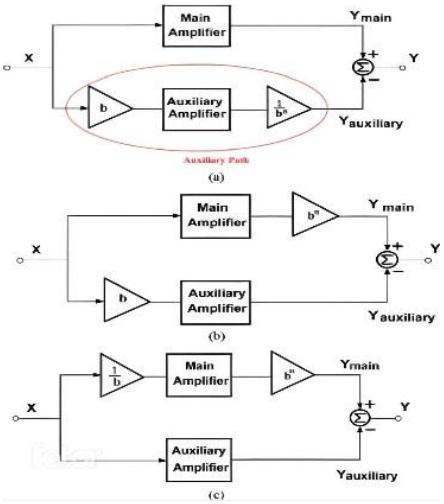

Figure 4.3: three illustrations of the linearization using feedforward method.

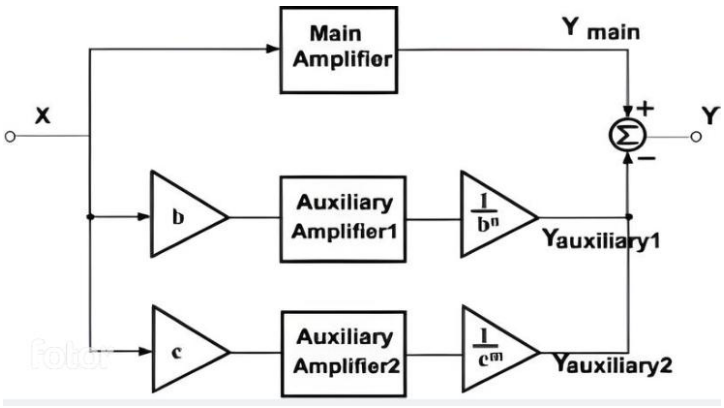

Figure 4.4: An enhanced method of feedforward linearization.

One instance of feedforward is the series of events seen in Fig. (4.3). Only a single kind of harmonic can be cancelled using the methods shown in Fig. 4.3. As shown in Fig. 4.4, two auxiliary paths could offer the additional degree of freedom required to simultaneously remove second- and third-order distortion. Regardless of the linearity of the amplifier, this universal feedforward technique improves linearity. It does, however, have a few shortcomings. For example

- It is frequently impractical to obtain highly linear, noiseless, and accurate scaling factors. As an example, the off-chip coaxial assembly utilized in is costly and unintegrable.
- Additional active components increase noise levels.
- Extremely susceptible to inconsistencies between the primary and secondary gain stages
- Since the auxiliary amplifier is a perfect replica of the main amplifier, power is doubled or tripled.

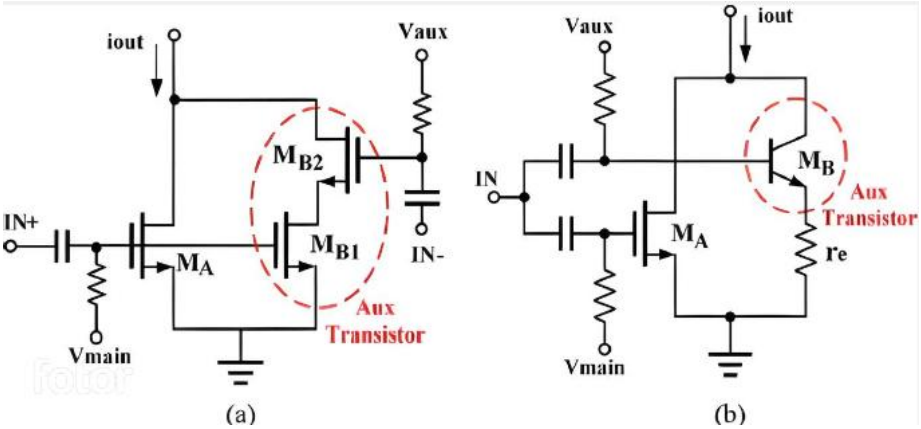

Figure 4.5: DS method. (a) Additional transistor works in triode region. (b) Use of a bipolar transistor.

4.4 Derivative Superposition(DS)

The derivative superposition (DS) technique is one specific use case for feedforward. By adding the third derivatives (g3) of the drain current from the main and auxiliary transistors, distortion is removed by the process known as "derivative superposition." A sign reversal of g3 indicates the shift from the weak to the strong inversion zones. Therefore, proper biassing results in zero g3. Not just at one bias voltage, but over a range of bias voltages, the linearity is improved. Because of the asymmetry in the positive and negative characteristics of g3, the cancellation window is tiny when there is only one auxiliary transistor. However, when there are more auxiliary transistors, the cancellation window increases at the expense of gain, NF, and input matching.
Figures 4.5(a) and 3.5(b) depict a triode region and a bipolar transistor, respectively, as possible auxiliary devices for the DS approach. As seen in Fig. 4.5(a), MB1 and MB2 are powered by differential input signals. The positive g3 peak of MB1, which is biassed in the deep triode region with the help of MB2, cancels out the negative g3 peak of the input transistor MA. As seen in fig. 4.5(b), in order to achieve maximal distortion cancellation, the positive g3 is supplied

by a bipolar transistor (MB), and the g3 is lowered to match the MA's by an emitter degeneration resistor.

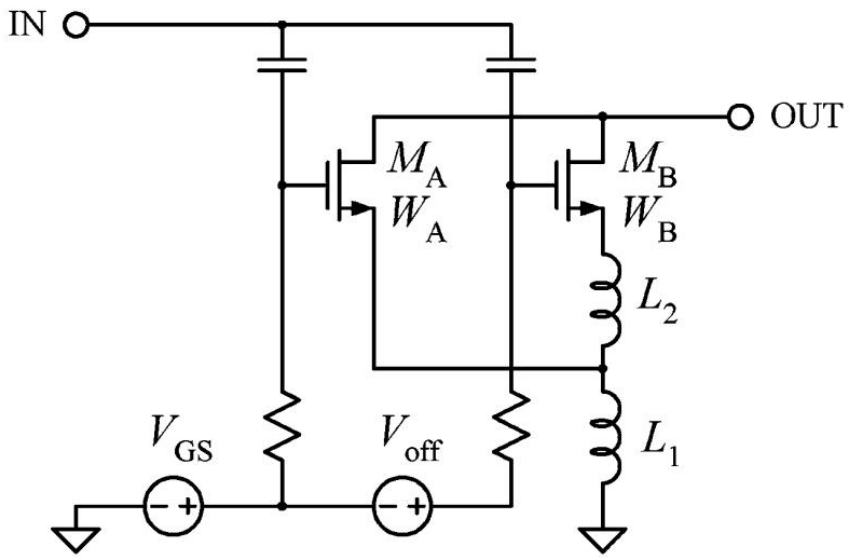

Figure 4.6: Derivative Superposition Techniques

4.4.1 Complimentary Derivative Superposition

The "complementary DS method" increases IIP3 without influencing IIP2 by using a pair of NMOS and PMOS. Fig. 4.7 shows the common-gate and common-source implementations. The ac current combiner in Fig. 4.7(b) might be a large coupling capacitor with a low impedance inside the signal bandwidth, or it could be a current mirror. The output current of NMOS/PMOS devices is expressed as follows: since the ac input signal is out of phase.

$$i_{dsn} = g_{1A}v_{gs} + g_{2A}v_{gs}^2 + g_{3A}v_{gs}^3$$

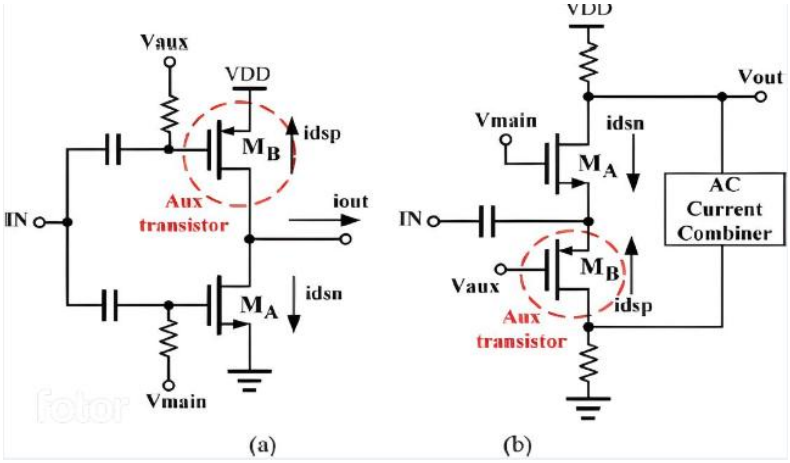

Figure 4.7: Complementary DS with (a) common-source configuration (b) common-gate configuration.

$$i_{dsp} = -g_{1B}v_{gs} + g_{2B}v_{gs}^2 - g_{3B}v_{gs}^3$$

$$i_{out} = i_{dsn} - i_{dsp} = (g_{1A} + g_{1B})v_{gs} + (g_{2A} - g_{2B})v_{gs}^2 + (g_{3A} + g_{3B})v_{gs}^3$$

The total transconductance increases, the IM2 term decreases because $g_{2A}$and g_{2B} havethe same sign, and the IM3 term decreases because g_{3A} and g_{3B} have different signs.

4.4.2 Modified Derivative Superposition

The vector diagram illustrated in Fig. 4.8 illustrates the concept of modified-DS. Even if the anti-parallel g3A and g3B sums in traditional DS are zero, IM3 is still present as a result of the g2A contributions. The updated DS approach spins g3B so that the vector of the combined g3A and g3B contributions is 180 degrees out of phase with the g2A contribution in order to obtain zero net IM3.
Fig. 4.8(a) shows a circuit realisation of the enhanced DS technique. Remember that the resulting g3B angle is determined by the value of L2. The gate noise of the weak inversion transistor (MB) is directly added to the gate noise of the main transistor (MA) due to their coupling. The MB's gate-induced noise is proportional to the drain current inverts. Input impedance matching is altered as well by (MB). Figure 4.8(b) illustrates a another approach to implementing the improved DS method. As MB is moved to the source of MA rather than being directly coupled to the input, the degradation in NF and input matching is minimised.

Limitations of the DS methods include following :
The weak-inversion transistor might not be able to reach a high enough frequency of operation.

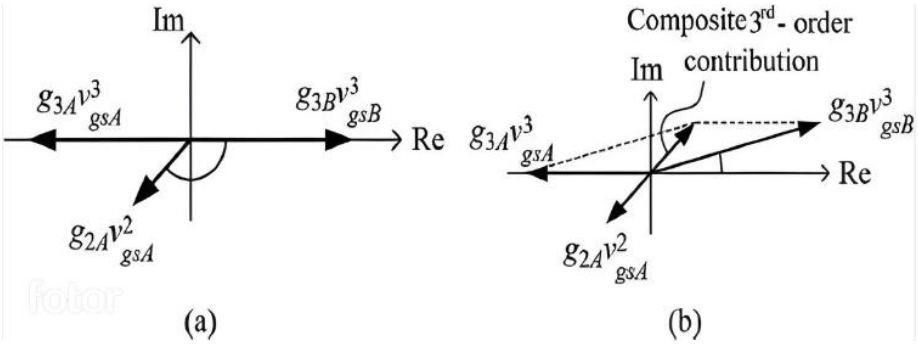

Figure 4.8: Vector diagram for the distortion components of (a) conventional DSmethod (b) modified DS method.

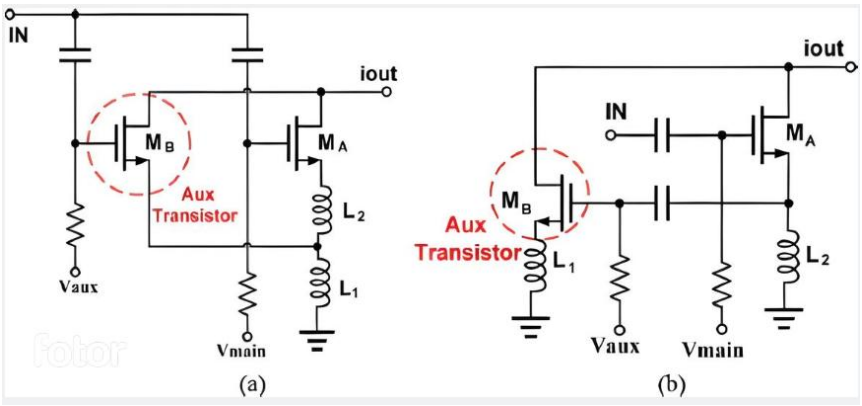

Figure 4.9: Circuit implementation of modified DS method.

- The distortion cancellation range of the weak-inversion transistor is severely constrained because it cannot tolerate strong signals and will either trip or burn out.
- Weak-inversion transistor models are typically imprecise, leading to a notable disparity between simulation and observation.
- When technology advances, the positive g3 peaks of triode-region transistors become less pronounced, making it more difficult to match their amplitudes to the negative peaks of main transistors.
- It can be challenging to match bipolar with MOS transistors or transistors operating in separate zones.

4.5 Cascode

In the Cascode topology, an interconnected source stage feeds a common gate stage. The development of the cascode topology was driven by the Miller effect, which will be covered in more detail in the next section. In a cascade structure, the input and the output are not closely related. Better separation between inputs and outcomes is therefore feasible.

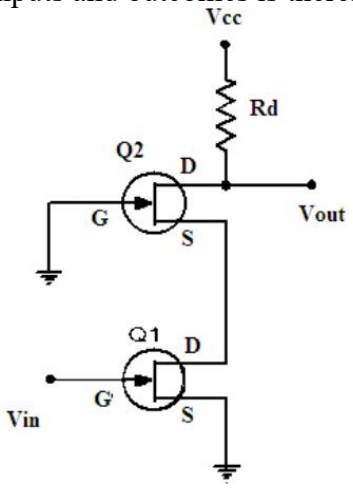

Figure 4.10: Simple cascode amplifier schematic diagram.

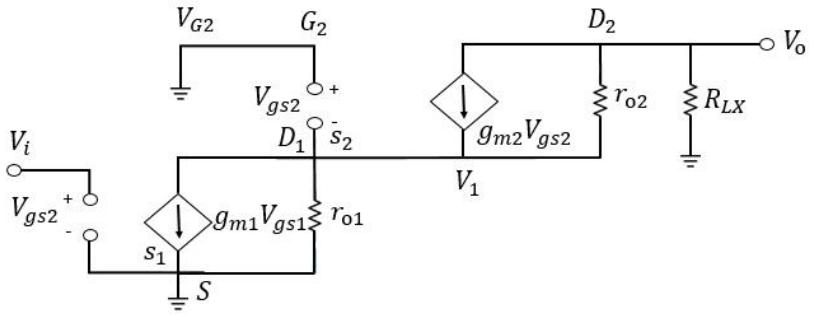

Figure 4.11: Simple cascode amplifier small signal model.

The miller effect causes the equivalent input capacitance of an inverting amplifier to increase, hence decreasing its bandwidth. An architecture with a cascode does not have this issue. In Figure 4.11 In the Cascode topology, a shared source stage feeds a common gate stage. The development of the cascode topology was driven by the Miller effect, which will be covered in more detail in the next section. In a cascade structure, the input and the output are not closely related. Better separation between inputs and outcomes is therefore feasible. The miller effect causes the equivalent input capacitance of an inverting amplifier to increase, hence decreasing its bandwidth. An architecture with a cascode does not have this issue. In Figure 4.10

4.5.1 Small Signal Analysis

A modest signal model of a straightforward cascode amplifier is displayed in Fig. 4.11. It is evident that the amplifier's modest signal voltage gain is

$$A_v = -g_{m1}r_{01}[1 + g_{m2}r_{02}] = -g_{m1}g_{m2}r_{01}r_{02}$$

$$R_0 = g_{m2}r_{01}r_{02}$$

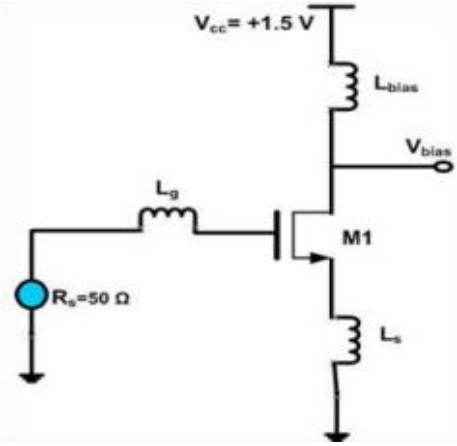

Figure 4.12: Simple cascode amplifier with inductive degeneration.

Tiny signal analysis shows that raising a cascode amplifier's gain requires raising the resistance of the load. In order to properly extract the gain from the cascode amplifier, we thus used a common source stage that came after the cascode stage and had an input resistance that was high enough.

4.5 2 Cascode Structure With Inductive Degeneration

Fig. 4.12 depicts a little portion of an inductively degenerated version of a basic cascode amplifier. This amplifier's input impedance is determined by:

$$Z_{in}(s)=s(L_g-L_{deg})+\frac{1}{sc_{gS}}+\frac{g_m Ldeg}{Cgs}$$

Inductive decay is one reason for input resistance. We can achieve input matching by placing inductance at the drain or source of the input stage. In order to completely eliminate the resistive component, our suggested design makes use of both inductive source degeneration and gate-to-drain feedback inductance.

4.5.3 Miller Effect

The amplification of capacitance between the input and output terminals by an inverting voltage amplifier causes an increase in the amplifier's equivalent input capacitance, which is known as the Miller effect. We can compute the Miller capacitance by considering an ideal inverting voltage amplifier with gain $-A_v$ and impedance Z linked between its input and output nodes. The resulting output voltage is $V_0= -A_vV_i$. Considering that the amplifier's input draws no current and that all of the input current flows via Z,

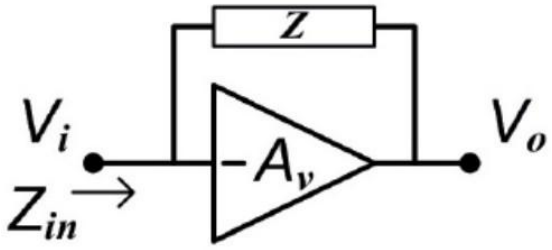

Figure 4.13: Miller effect explained

we have:

$$I=\frac{v_i-v_0}{Z}=\frac{v_i(1+A_v)}{Z}$$

The input impedance of the circuit is :

$$Z_{in}=\frac{v_i}{I_i}=\frac{Z}{1+Av}$$

If Z represents a capacitor with Z impedance Z=1/(sC) ,the resulting input impedance is Z_{in}=1/(sC).Here

$$C_M = c(1 + A_v)$$

The symbol for Miller capacitance is C_M. Although the Miller effect is most frequently linked to capacitance, any impedance that is connected between the amplifier's input and another node that is exhibiting gain could alter the input impedance. Active devices such as transistors and vacuum tubes have a parasitic capacitance between their input and output, which causes a Miller capacitance at high frequencies, which significantly limits their gain.

4.5.4 Advantages of Cascode Topology

Better Linearity and Noise Performance: In a single CS structure, linearity and noise performance decline based on the matching technique. A single CG structure, however, performs better in terms of noise and linearity than a CS stage. The best elements of both types are thus combined in cascode architecture.

Stability: The robustness of the cascode's design is enhanced by the physical and electrical separation of input and output. Because the source and drain voltages are nearly constant, nothing can be fed back into the gate of the CS stage. Furthermore, the CS stage's source and gate voltages are quite stable. For this reason, the only two nodes that are important are input and output. The distance between two transistors and the core constant voltage connections divide these both physically and electronically.

Mitigation of Miller Effect: The common source stage is an inverting amplifier. Common gate stage in a cascaded common source amplifier acts as a load. The source of the CG stage, which is maintained at the operating frequency, keeps the drain of the CS stage at a practically constant voltage. Lowering the gain is the result of the CG stage's low input impedance to the CS stage. Miller has such a diminished impact.

High Gain and Bandwidth: The gain in the CS stage is lowered to minimise the miller effect. But the lost gain is made up for in the CG stage. We can expect a significantly greater bandwidth since there is less negative feedback and less gain-induced multiplication of the input stray and parasitic capacitance.

Reverse Isolation: Input and output in a cascade structure are not connected directly. This allows one to acquire the necessary reverse isolation parameter for an amplifier.

Improved Power Efficiency: In some cases, cascode amplifiers can achieve improved power efficiency compared to other configurations. This is particularly true in applications where high voltage swings and low distortion are required simultaneously.

Higher Voltage Swing: Cascode amplifiers can handle higher voltage swings at the output compared to single-stage amplifiers. This makes them suitable for applications requiring larger signal swings without distortion.
Enhanced Output Impedance: The cascode configuration provides a higher output impedance compared to a single-stage amplifier. This can be advantageous in driving loads with varying impedances without significantly affecting the performance of the amplifier.

4.6 Noise Cancellation

As seen in fig. 4.14, noise cancellation parallels the CG(MA) and CS(MB) stages. The voltage at node "IN" powers the circuit. One way to represent the nonlinearity of (MA) is as a current source that is controlled by both V_{gs} and V_{ds} between the drain and source. As a result, at the output, the signal is added while the channel thermal noise and flow distortion across the CG and CS routes are eliminated. For noise cancellation to occur, $V_x = V_y$, that is,

$$g_1, M_A R_A = g_1, M_B R_B (differentialoutput)$$

$$g_1, M_{B1} R_S = g_1, M_{B2} R_A (single - endedoutput)$$

It should be noted that earlier solutions could only adjust for g_m nonlinearity; this technique can negate all intrinsic distortion created by MA, including both g_m and g_{ds} nonlinearity. The residual nonlinearity, which consists of two terms, is dominated by the distortion caused by MA after the distortion from MA has been cancelled.

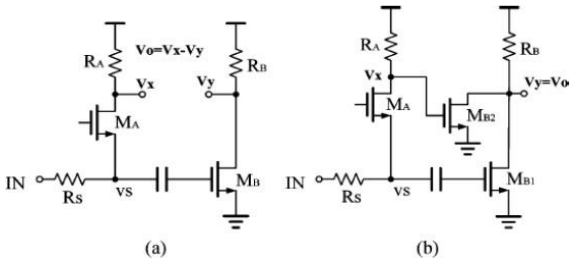

Figure 4.14: Noise cancellation. (a) Differential output. (b)Single ended output.

- M_B's intrinsic third-order distortion.
- Second-order interaction originating from the CG-CS cascade

Optimal biasing of M_B or employing complementary DS could further improve the linearity.

4.7 Post Distortion

Similar to the DS approach, the post-distortion (PD) methodology cancels the nonlinearity of the primary device by utilising the nonlinearity of an auxiliary transistor. The PD approach, however, is more advanced in two ways.

- To reduce the influence on input matching, the auxiliary transistor is connected to the main device's output rather than directly to the input.
- More reliable distortion cancellation is achieved when all transistors are operating at saturation.

Three implementations and a conceptual design of PD are shown in Fig. 4.15. Both the second- and third-order distortion effects are partially cancelled by the auxiliary transistor MB, which replicates the main transistor MA's nonlinear drain current by tapping voltage v2. One way to r

$$i_A = g_{1A}v_1 + g_{2A}v_{12} + g_{3A}v_1$$

$$i_B = g_{1B}v_2 + g_{2B}v_{22} + g_{3B}v_2$$

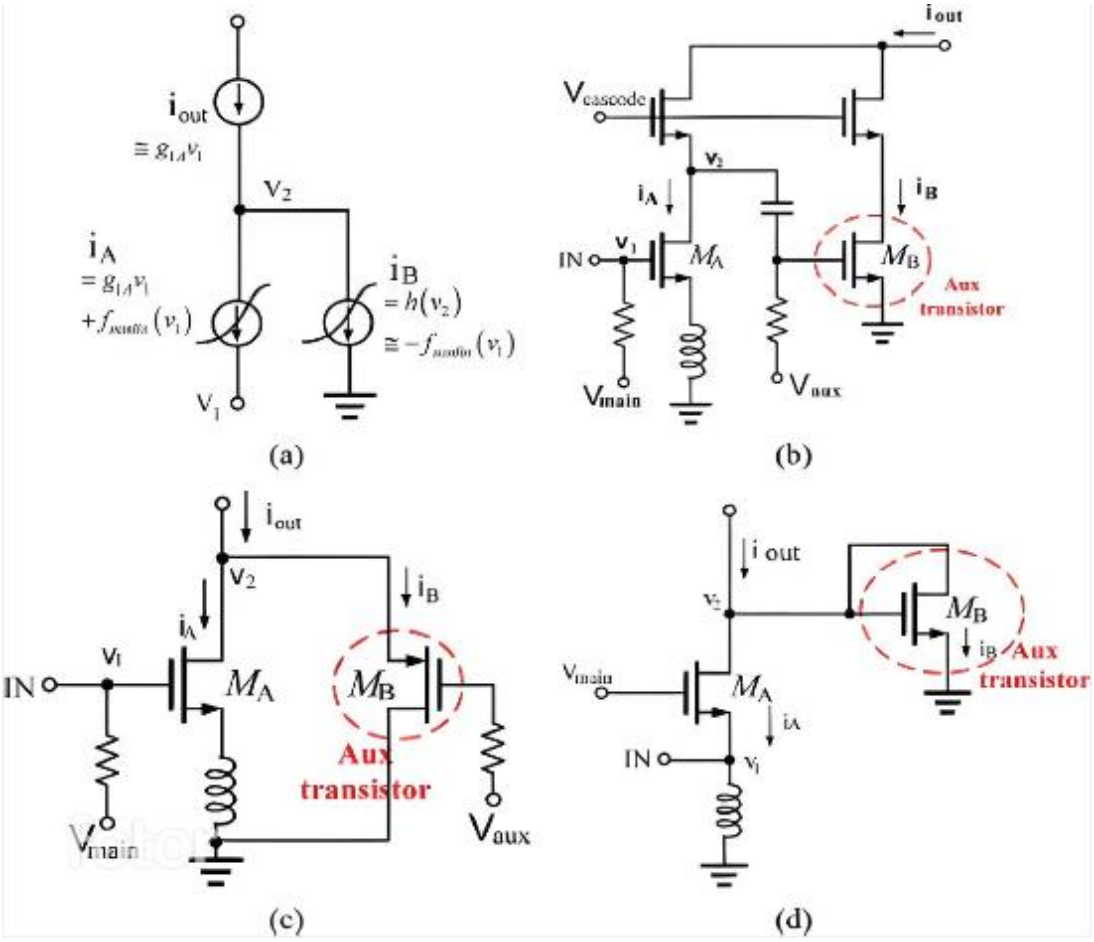

Figure 4.15: Post distortion. (a) Conceptual view. (b)(c)(d) Circuit implementation

Next, Suppose v_2 is related to v_1 by

$$v_2 = -b_1v_1 - b_2v^2 - b_3v_1{}^3$$

whereb_1- $b_3$are generally frequency dependent and can be extracted from simulation. In Fig. 3.14(a), the cascode devices were assumed to be ideal current buffers. The two nonlinear currents $i_A$and i_B sum at node v_2, yielding i_{out}:

$$i_{out} = i_A+i_B = (g_{1A}-b_1g_{1b})v_1+(g_{2A}-b^2g_{2B}-b_2g_{1B})v^2+(g_{3A}+b^3g_{3B}-g_{1B}b_3-2g_{2B}b_1b_2)v^3$$

In the PD method, both the main and auxiliary transistor operate in saturation with the same $g_{1,2,3}$ polarity . Hence, Partially cancels the linear term as well. However ,it does not substantially degrade the gain/NF is designed to be more nonlinear than M_A

Chapter 5

Proposed Architecture

The objective of most architectures described in the literature is to reduce second and third order intramodulation distortion. Suppression of terms higher than the third order, however, is still a problem. It is crucial to remember that linearity affects gain and vice versa when designing a low-noise amplifier. As such, the design that is being discussed focuses on attaining a sufficient gain while maintaining superior linearity. Three linearization methods, including robust derivative superposition and post-linearization, are used in the suggested topology. In order to achieve better linearity performance, our proposed architecture additionally aims to cancel out the nonlinearity caused by the cascode structure's shared gate stage mosfet.

5.1 Circuit Design

Figure 5.1 shows the proposed circuit architecture. It consists of an inductive source degenerating cascode structure. Because it provides highest transconductance gain, minimum noise penalty, and simultaneous impedance matching, inductive source degeneration is typically chosen in RF circuit design. Three distinct nonlinearity suppression methods are incorporated into the amplifier. They consist of:

- Robust Modified Derivative Superposition Method
- Post Linearization Technique
- Common Gate Stage Mosfet Linearization

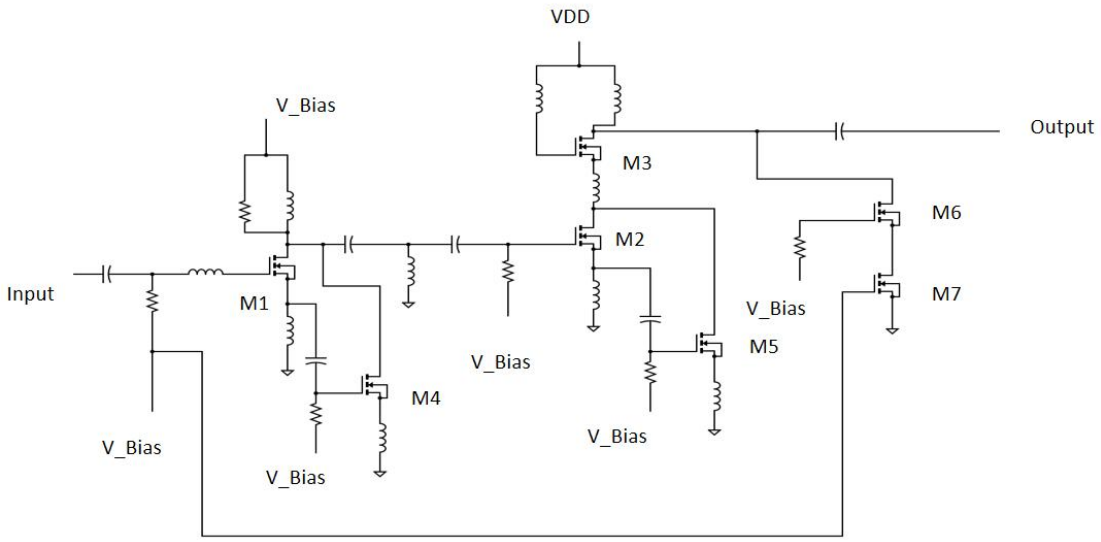

Figure 5.1: Proposed Architecture

With reference to the picture, the amplifier's cascode stage consists of up of M1, M2, and M3. In order to match the input and output port impedance while minimizing the noise figure, this first stage comprises of multiple matching networks. The robust Modified derivative superposition branch is represented by the M4 and M5 mosfets, while the postlinearization approach is used by M6 and M7.

5.2 Input Matching Network

Fig. 5.2 shows the conventional cascode form with source degeneration. The structure's small signal equivalent circuit is shown in Fig. 4.3. The input impedance of 50 ohms that was observed at the input port can be expressed using the following simplified equation, which does not account for the gate resistance or any other parasitic capacitance other than the gate-source capacitance .

$$Z_{in}=jw(L_g+L_s)+\frac{1}{jw(C\ gs1+Cex)}+\frac{gm1}{Cgs1+Cex}$$

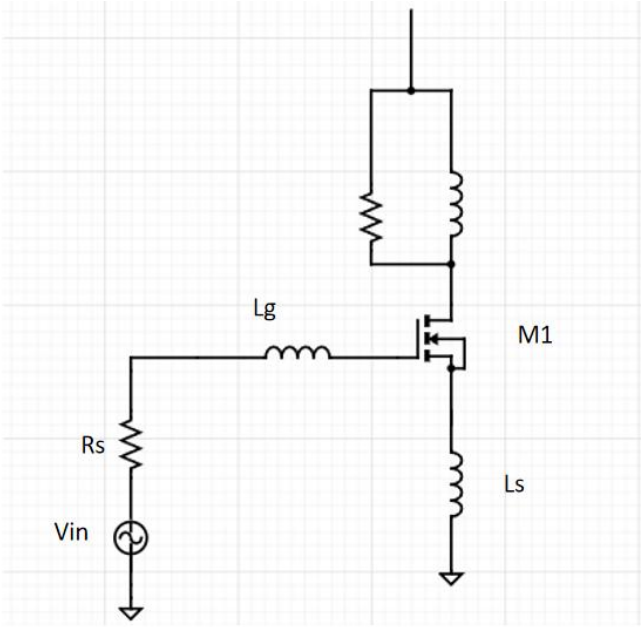

Figure 5.2: The Cascode amplifier with inductive degeneration

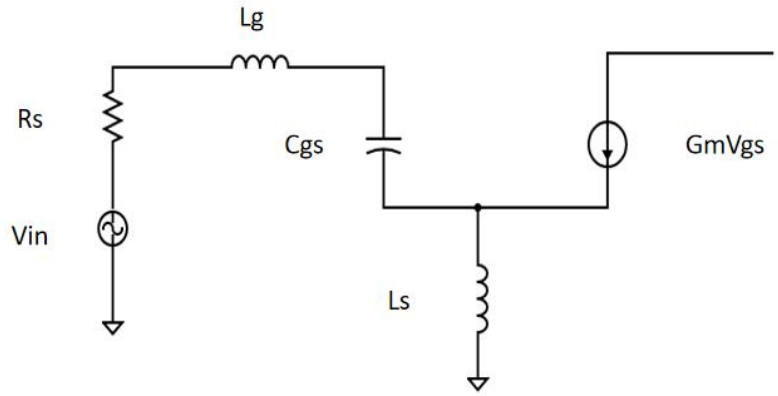

Figure 5.3: Small signal equivalent circuit for the driving circuit section of Fig. 5.2.

where Cgs1 and gm1 stand for the gate-to-source capacitance and intrinsic transconductance of the device, respectively. Ls is the source degeneration inductor used for matching, Ld is the drain inductor that provides output resonance with load capacitance and is essential to producing amplification, and Lg is the gate inductor that is used to filter away the effect of input capacitive elements . The imaginary components of the impedance should cancel each other out at the remainder frequency in order to match the input impedance to precisely 50 ohms. Equation 5.1 gives us three degrees of freedom to accomplish this. It is made easier to eliminate the imaginary components from the input impedance by the degeneration inductor Ls. The genuine portion, however, needs to be matched to precisely 50 ohms, thus there are one constraints on the right Ls selection. Two counter this: the intrinsic gate to source capacitance Cgs1 placed. This contributes to a significant reduction in the size of Ls and provides us with additional design freedom for the matching circuit.

5.3 Inter stage Matching

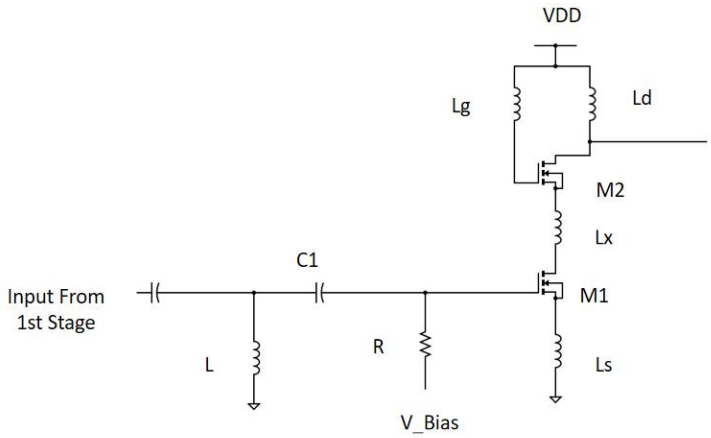

Figure 5.4: Cascode amplifier with interstage matching

It is important to maximize the power transfer between the two stages of the cascode amplifier. Therefore, an interstage matching network is carefully designed. To achieve maximum power transfer, the input impedance of M2 should have a value equal to the complex conjugate of the driver mosfet M1. In our proposed architecture, the network is realized by the series inductor . The value of the components has to be chosen carefully so that at the resonant frequency, the impedances match perfectly. This introduction of an interstage matching network facilitates the suppression of signals at undesirable frequencies, consequently improving the linearity of the amplifier.

5.4 Output Matching

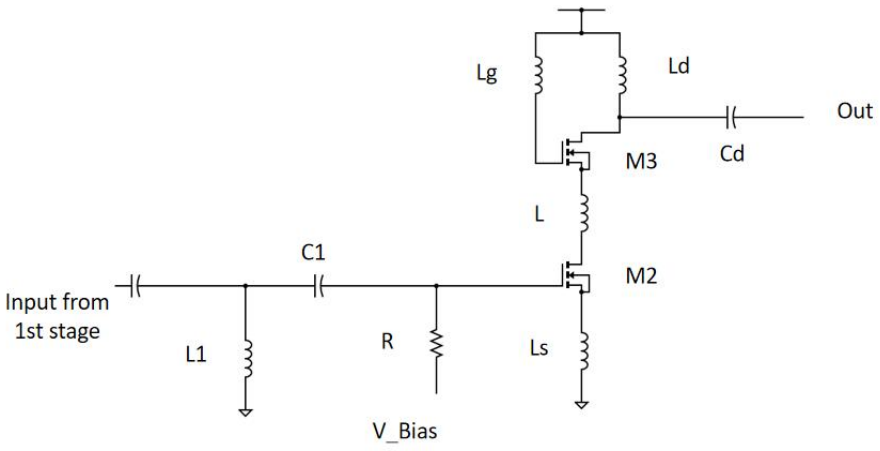

Figure 5.5: Cascode amplifier with all the matching networks

The mosfet M3's drain is where the cascode amplifier's output is obtained.500 ohm is the load that we have chosen. It is necessary to match the output impedance to the 500 ohm port resistance in order to guarantee maximum power transfer to the output port. A capacitor has also been placed in front of a load.

5.5 Linearization Techniques

There are various benefits to the basic cascode structure. They are as follows:

- It lowers the miller capacitance, making input and output impedance matching easier;
- It offers strong isolation between input and output ports.
- Because of its enhanced output impedance, the cascode structure yields a low noise figure and offers very high gain.

Nonetheless, the lack of linearity of the cascode structure is one of its biggest drawbacks. Most of the observed nonlinearity can be attributed to the current's third-order fluctuation. Furthermore, the second order aberrations compound and further diminish the linearity. Consequently, further linearization of the cascode structure is necessary.

5.5.1 Robust Modified Derivative Superposition

Modified derivative superposition techniques improve the performance of Low-Noise Amplifiers (LNAs) by providing a more comprehensive analysis of the amplifier's behavior, especially in dynamic scenarios. By considering not only the initial conditions and the input signal but also its derivatives, these techniques offer deeper insights into how the LNA responds to rapidly changing or multi-frequency inputs. This deeper understanding aids in optimizing crucial performance parameters such as bandwidth, linearity, and noise figure. LNAs are often utilized in communication systems where signals may vary rapidly or contain multiple frequency components, making the insights gained from modified derivative superposition invaluable for ensuring optimal performance in such applications.By biassing at a gate source voltage where the third-order fluctuation in current is zero, a fet can be made linear. The most effective biassing method is, however, susceptible to process and temperature variations. Consequently, in order to eliminate the nonlinearities, alternative methods must be investigated.
In our proposed architecture, most of the nonlinear behaviour is caused by the CS stage mosfet M1. A derivative modified superposition branch was added to improve the circuit and get rid of the third-order non-linearities. The IIP3 is less susceptible to bias in this method, and achieving zero gm requires navigating a bias window rather than a bias point. Where gm is defined as

$$G_m'' = \frac{\mathrm{d}^3 i_d}{dv g_S^3}$$

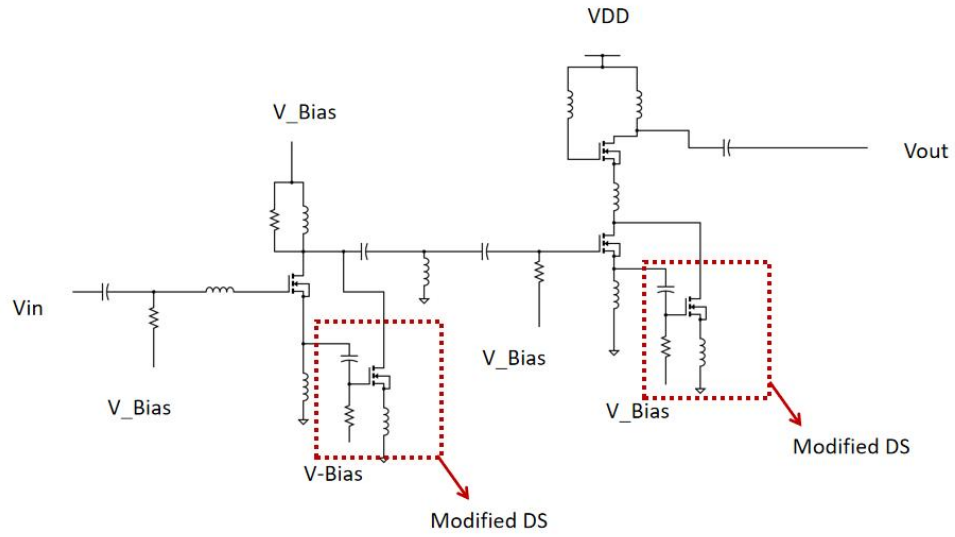

Figure 5.6: Cascode amplifier with robust Modified derivative superposition branch

5.5.2 Post Linearization

Post-linearization techniques in Low-Noise Amplifiers (LNAs) are crucial for improving amplifier performance by mitigating non-linear distortions that degrade signal quality. These techniques, applied after the amplification stage, enhance linearity, reduce intermodulation distortion, and preserve signal fidelity. By compensating for non-linearities, they extend the dynamic range, optimize system performance, and ensure accurate signal representation in applications such as wireless communication and radar systems.

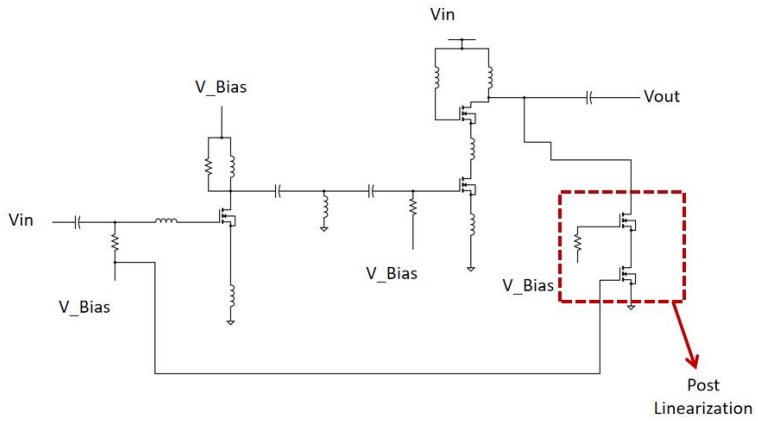

Figure 5.7: Cascode amplifier with Post Linearization Techniques

5.5.3 Linearization The cascode MOSFET

Up till now, nonlinearity caused by CS stage MOSFET M1 ,M2has been our sole worry. Nevertheless, nonlinearities resulting from the CG stage MOSFET (Cascode MOSFET) become significant at high gain and frequency. Because of the amplifier's extremely high gain, the

MOSFET M3 in our suggested architecture is the cas-code mosfet that causes some nonlinearity. The nonlinear change of the drain current caused by cascode is shown in Figure 5.10.

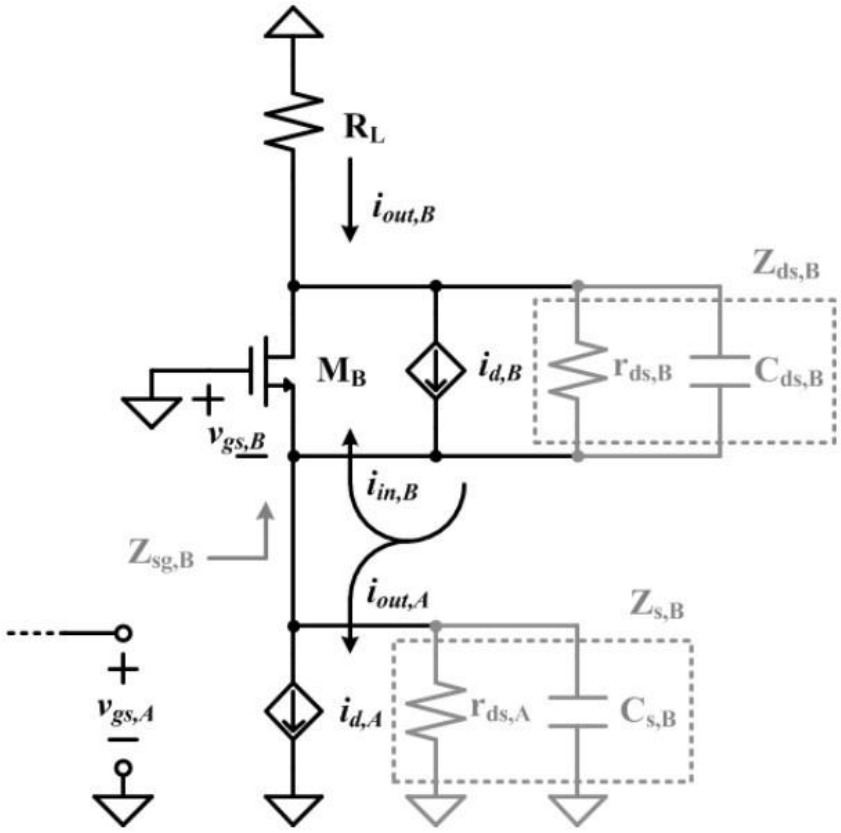

Figure 5.8: Circuit diagram of nonlinearity analysis of the CG stage in the cascode LNA.

mosfet M_B. The CS stage is essentially a voltage controlled current source. The drain current of CS stage is fed to the CG FET M_B. Now the drain current can be modeled as:

$$i_{d,B}=g_{m1,B}V_{gs,B}+g_{m2,B}V^2_{gs,B}+g_{m3}V^3_{gs,B}$$

This linearization method is almost similar to the robust derivative superposition branch explained. The final architecture is shown in Fig 4.11 which achieves superior gain and linearity due to the careful choice of the bias voltages and MOSFET size.

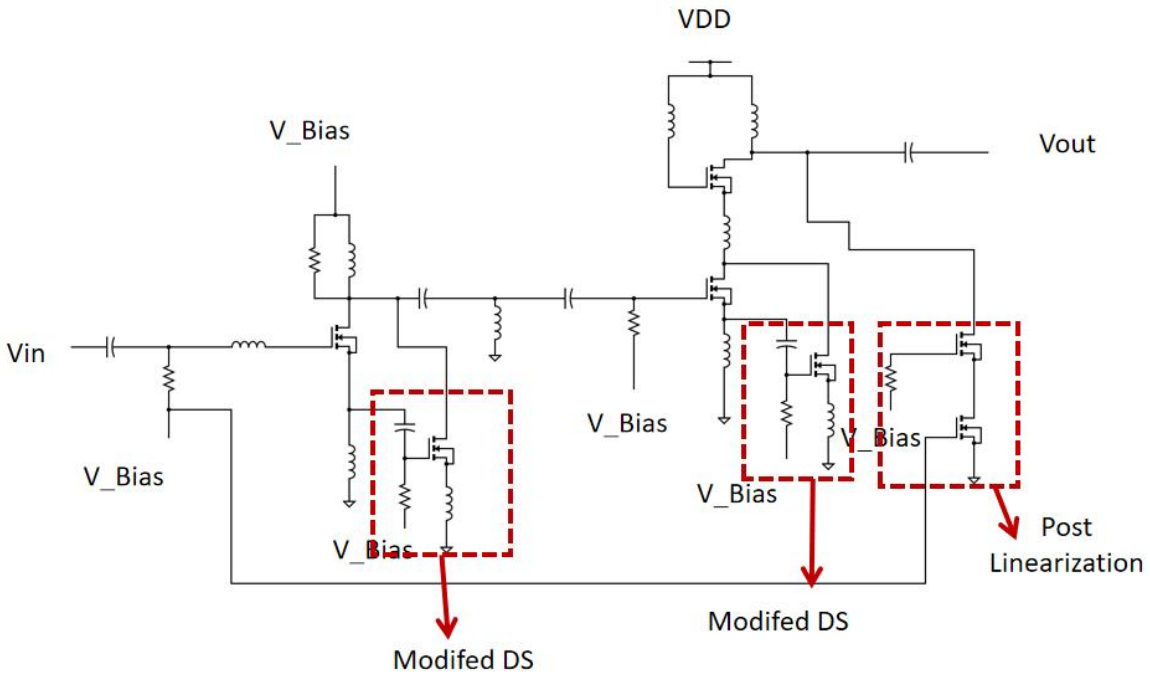

Figure 5.9: Final architecture

Chapter 6

Simulation Results and Discussion

We have utilized Cadence Virtuoso software in combination with 90 nm process technology for simulating these circuits. There are some particular reason for choosing this software for simulation. It is a widely used standard tool for analog circuit design, so using an established platform adds credibility. In addition, it offers an integrated environment that includes schematic capture, layout design, and verification. It also has the ability to perform accurate modelling of the non linearities like noise

6.1 2 Stage CS Cascode Topology

6.1.1 S parameters

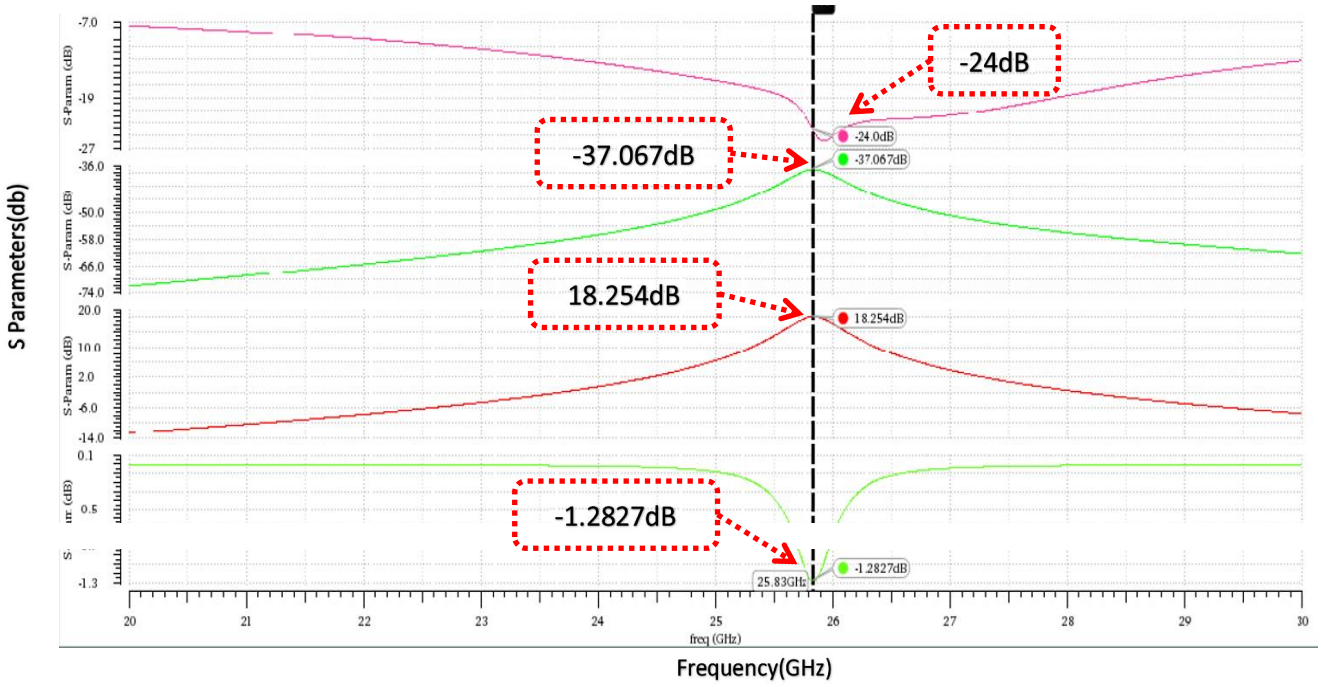

Fig 6.1.1 : S parameters vs Frequency of 2 stage Cascode LNA

Here we can see 4 different parameters for 2 Stage Cascode LNA. The 1st parameter is input reflection coefficient(S11) and it value is -24 dB.The 2nd parameter is reverse isolation coefficient (S12) and its value is -37.067dB.The 3rd parameter is Forward transmission gain (S21) and its value is around 18.254dB and the last parameter is Output reflection coefficient and its value is around -1.2827dB.All this parameter are measured at 25.83GHz.

6.1.2 Noise Margin

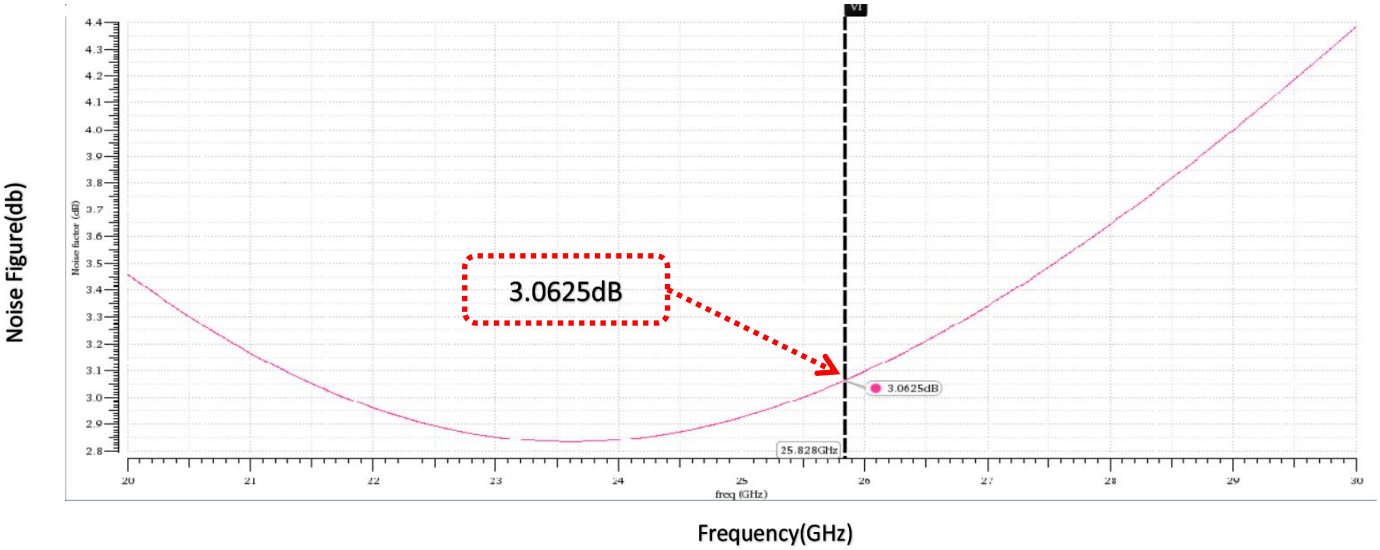

Fig 6.1.2 :Noise Figure(db) Vs Frequency for 2 stage Cascode LNA

Here the noise figure is around 3.0525dB at the frequency of 25.83GHz. For 5G application ,the noise figure must be within 2dB to 7dB.

6.1.3 IIP3

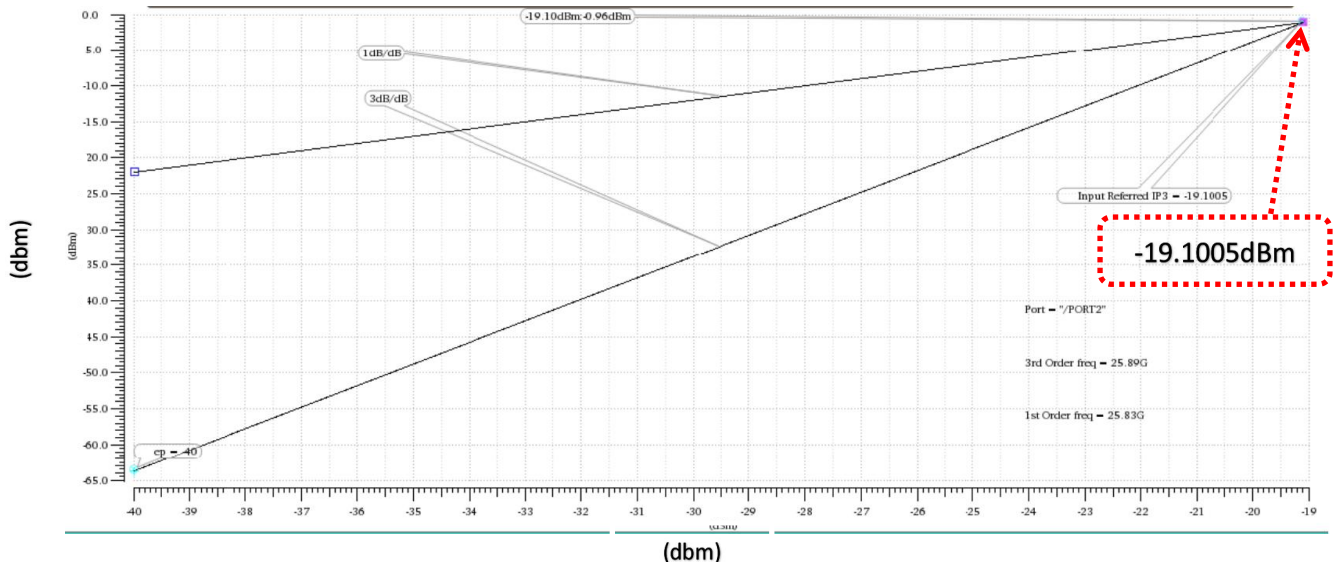

Fig 6.1.3 :Ipn curves for 2 stage Cascode

Here the 3rd order intercept point (IIP3) is -19.1005dBm which very small .But for 5G application, we need high linearity .To achieve that linearity we have used different techniques which has need described below.

6.2 2 Stage Cascode Topology with DS in first stage

6.2.1 S parameters

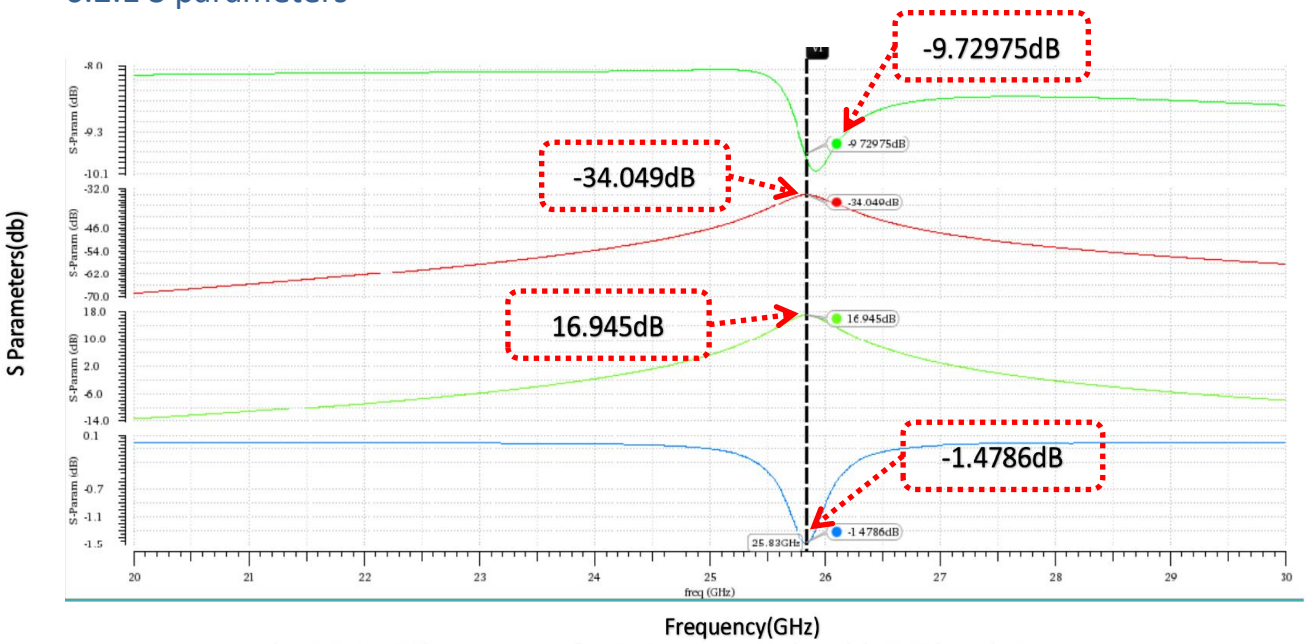

Fig 6.2.1 : S Parameters for 2 stage cascode with DS in 1st stage

Here we can see 4 different parameters for 2 Stage Cascode LNA. The 1st parameter is input reflection coefficient(S11) and it value is -9.72975 dB.The 2nd parameter is reverse isolation coefficient (S12) and its value is -34.049 dB.The 3rd parameter is Forward transmission gain (S21) and its value is around 16.945 dB and the last parameter is Output reflection coefficient and its value is around -1.4786 dB.All this parameter are measured at 25.83GHz. Here ,due to use of DS method, the gain has reduced a little bit around 2 dB .

6.2.2 IIP3

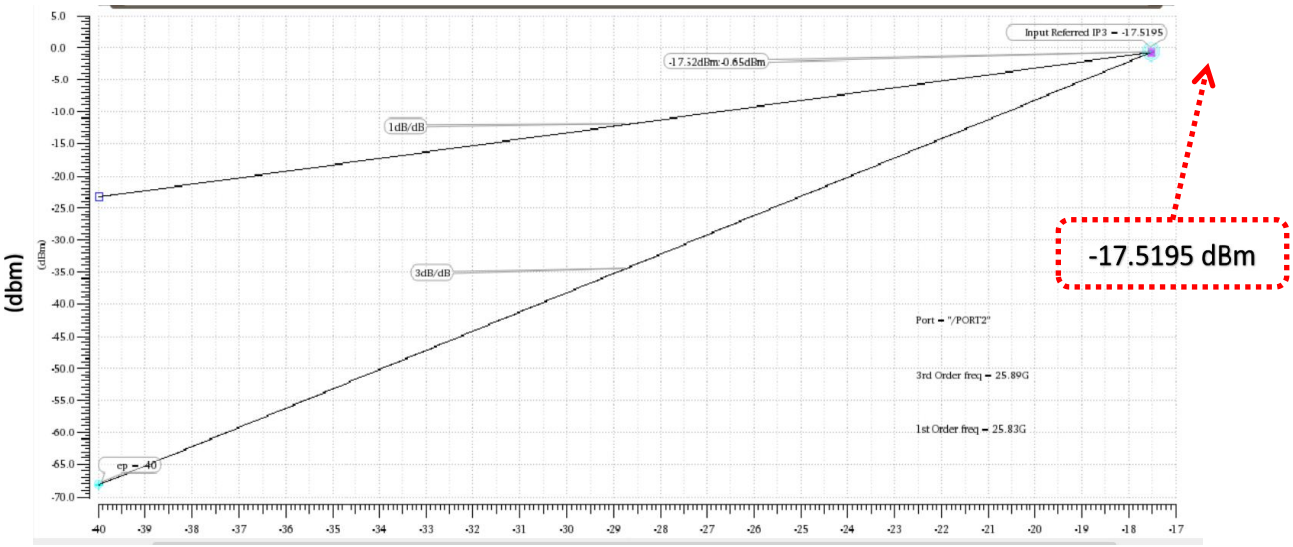

Fig 6.2.2 :Ipn curves for 2 stage cascode with DS in 1st stage

Due to use to DS method in 1st stage ,the 3rd order inteecept point has moved to -17.5195dBm. So ,we can say, the linearity has increased by around 2dBm.

6.3 2 Stage CS Cascode Topology with DS in both Stages

6.3.1 S Parameters

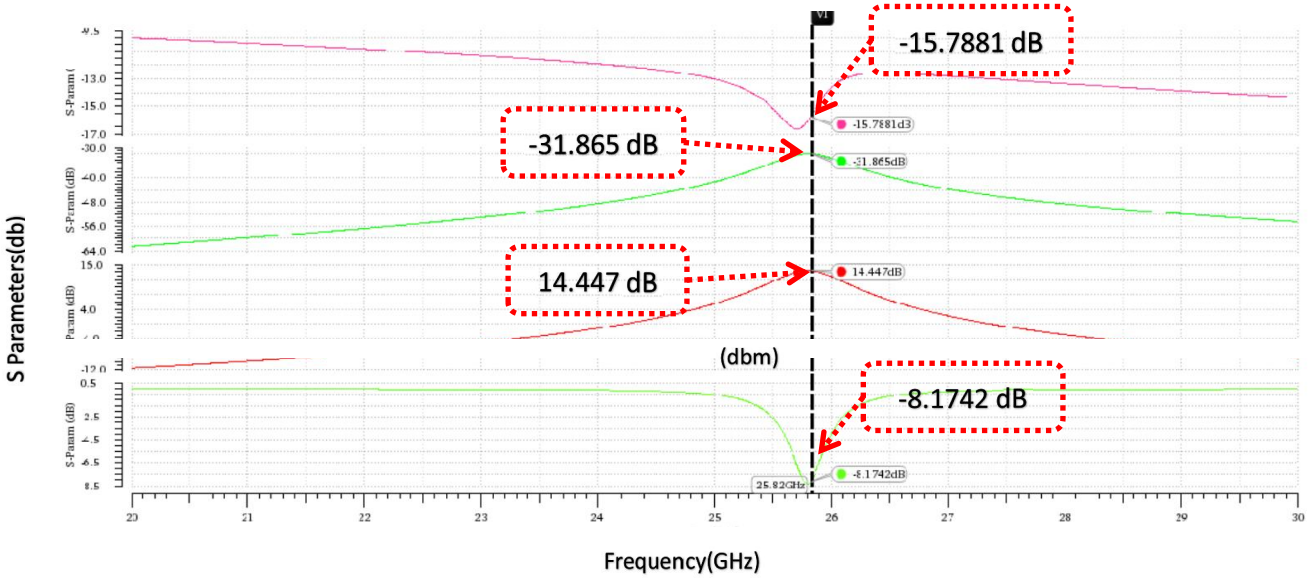

Fig 6.3.1 : S Parameters for 2 stage cascode with DS in both stage

Here if DS method on both stages then , the transmission coefficient is around 14.447 dB.So the gain has further reduced . But it is still under the range of 5G application(10dB to 20dB).The other parameters are also in the reasonable ranges.

6.3.2 IIP3

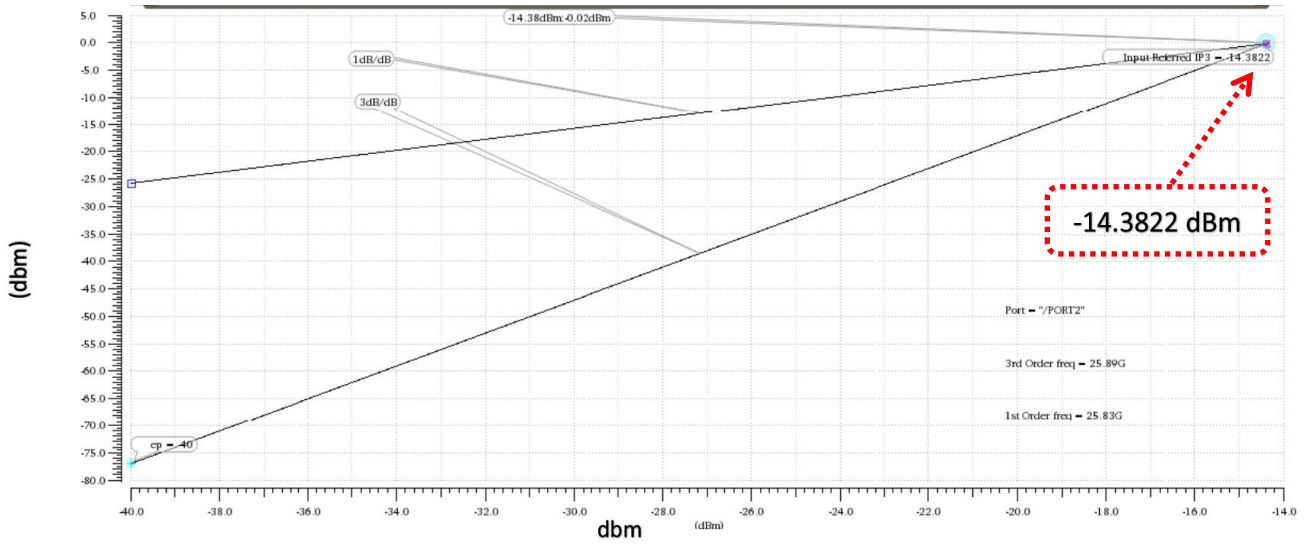

Fig 6.3.2 :Ipn curves for 2 stage cascode with DS in both stage

Due to use of DS method in both stages, the 3rd order intercept point has moved to -14.3822dBm. So the linearity has improved around 3 dBm which is the 1st requirement for 5G application. However we can increased the gain by cascading technique.

6.4 2 Stage CS Cascode Topology With DS and Post Distortion

6.4.1 S Parameters

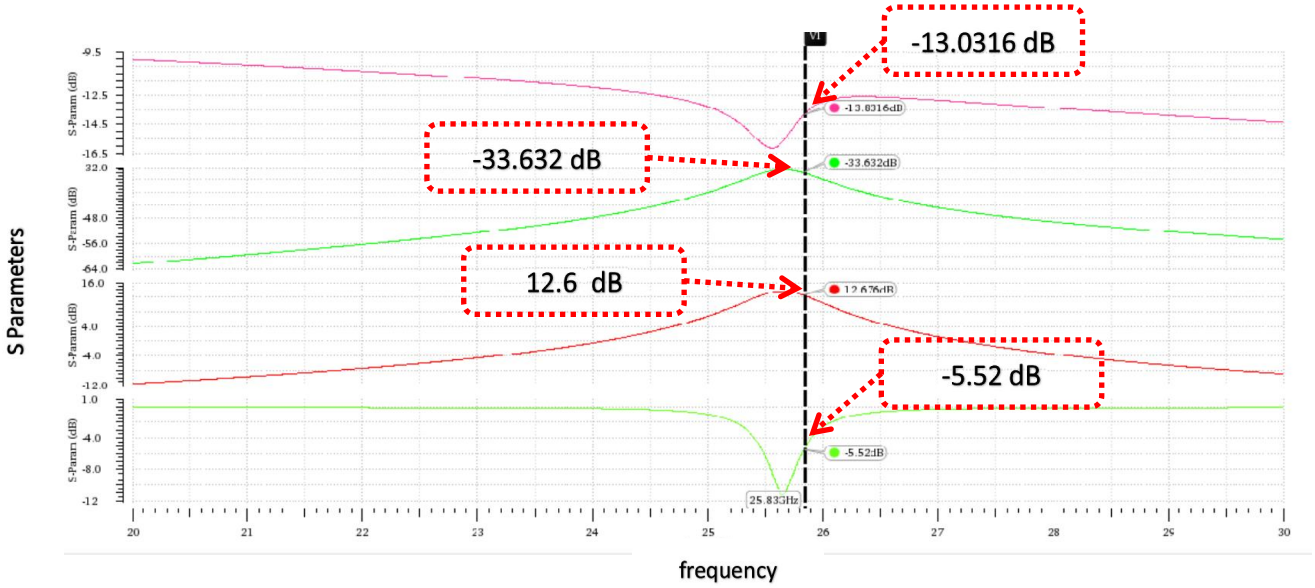

Fig 6.4.1 : S Parameters for 2 stage cascode with DS in both stage and Post distortion

Here the transmission coefficient gain(S21) is around 12.6dB which has been reduced due to use of DS method on both stages and post distortion network at the second stages.But it is still in the reasonable range for 5G application.

6.4.2 IIP3

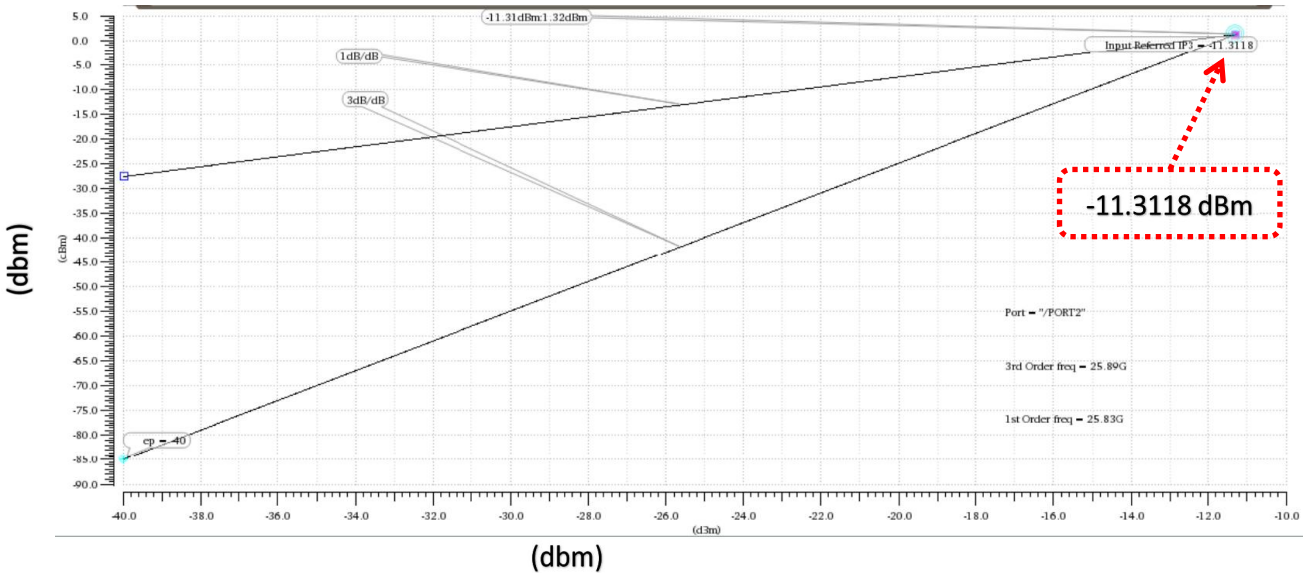

Fig 6.4.2 :Ipn curves for 2 stage cascode with DS in both stage and Post distortion

Here, the 3rd order intercept point value is around -11.3118dBm which is increased due to use of DS method on both stage and post distortion network on the 2nd stage.The IIP3 has been improved by around 3dBm which is desired to have a high speed data transfer rate for 5G Applications.

6.5 2 Stage CS Cascode topology With Modified DS and Post Distortion

6.5.1 S parameters

Gain(S21)

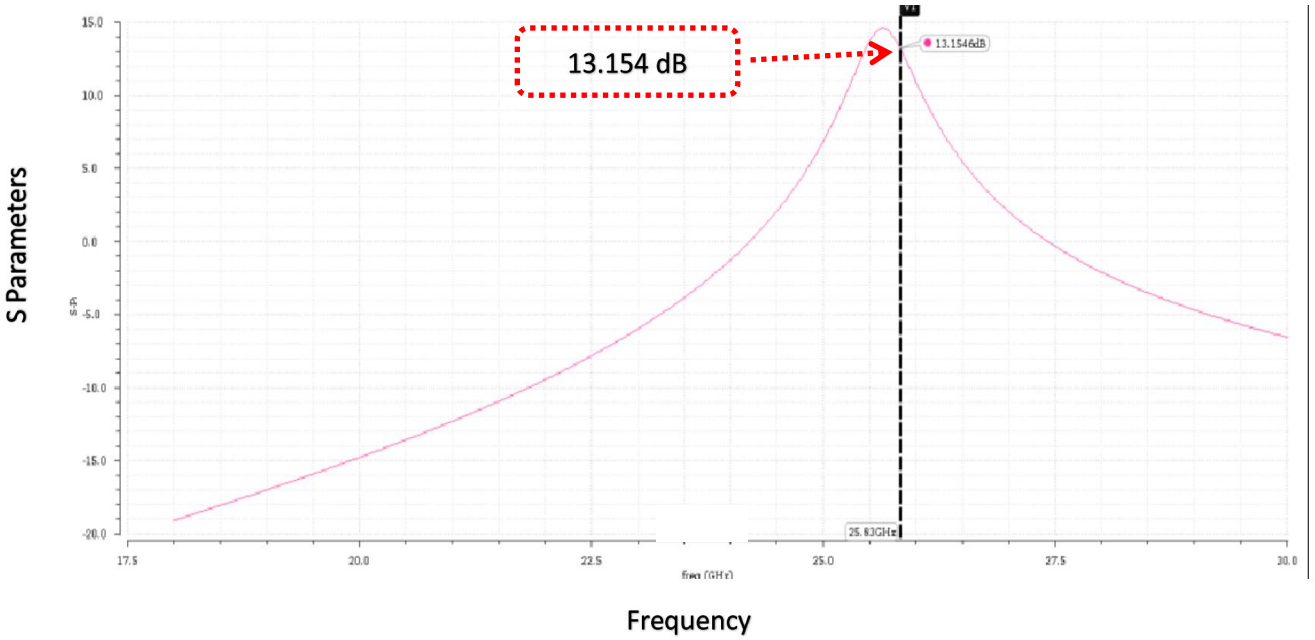

Fig 6.5.1.1 : Gain for 2 stage cascode with Modified DS in both stage and Post distortion

Here we have replaced the DS method by Modified DS method that actually increase the gain and the linearity curve. In previous DS method the gain is around 12.6dB ,which has been increased by the Modified DS method and the value is 13.154dB.The reason for increasing the gain in modified DS is the higher Vgs.In convention DS method the Vgs is comparatively small ,so the gain is also small as gain is proportional to Vgs.But I Modified DS method , the Vgs value is comparatively is vary high which actually increased the gain. In summary ,we can say ,modified DS method has increased the gain by around 1dB.

S11,S12,S22

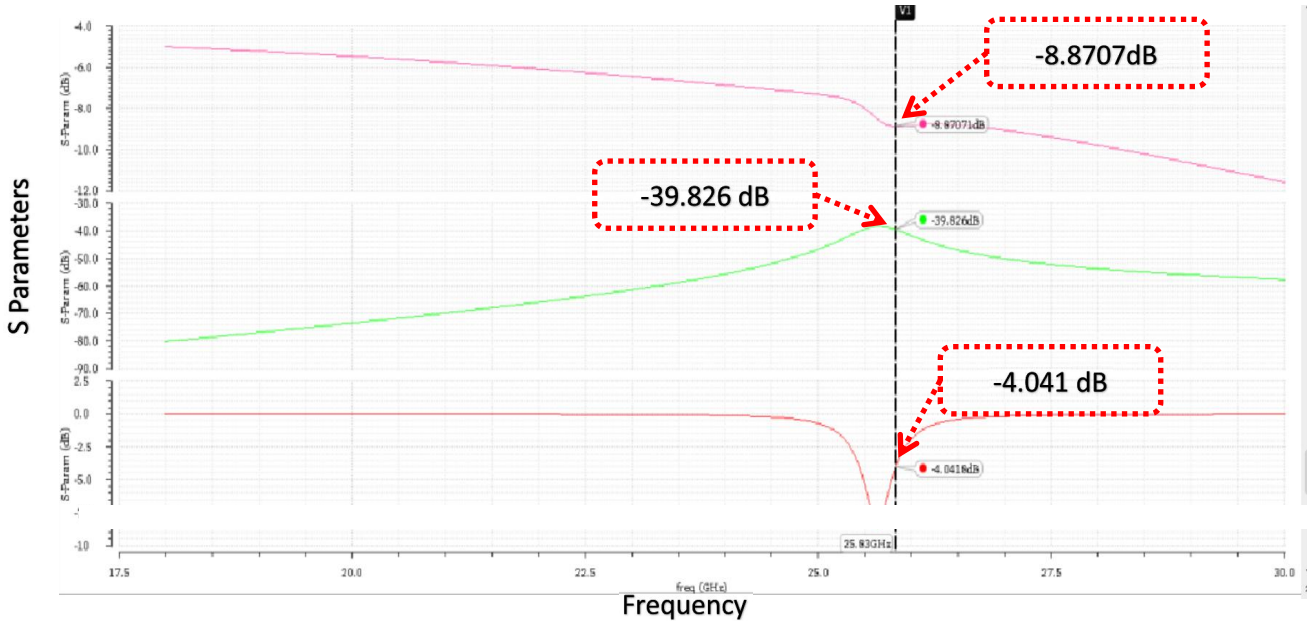

Fig 6.5.1.2: S Parameters for 2 stage cascode with Modified DS in both stage and Post distortion

Here we can see 3 different parameters for 2 stage cascode with Modified DS in both stage and Post distortion. The 1st parameter is input reflection coefficient(S11) and it value is -8.8707 dB.The 2nd parameter is reverse isolation coefficient (S12) and its value is -39.826 dB.The last parameter is Output reflection coefficient and its value is around -4.041 dB.All this parameter are measured at 25.83GHz. Here all three parameters are in the reasonable range of 5G application.

6.5.2 IIP3

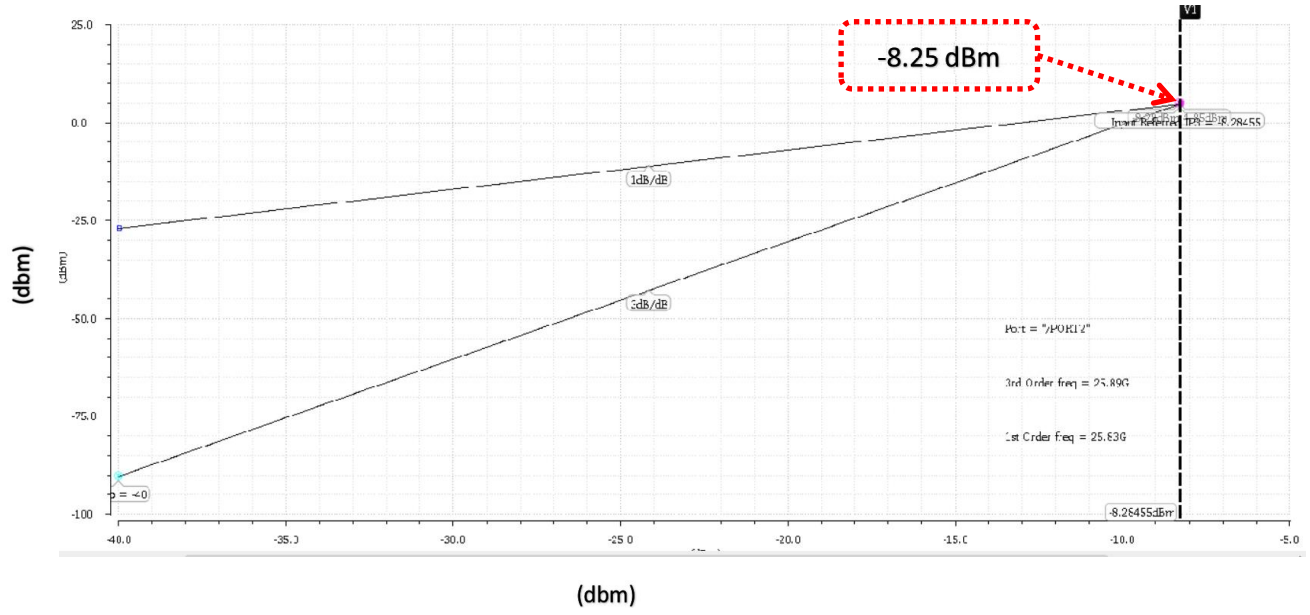

Fig 6.5.2 :Ipn curves for for 2 stage cascode with Modified DS in both stage and Post distortion

Here the 3rd order intercept point is around -8.25dBm which has been increased due to use of modified DS method in placed of conventional DS method.In conventional DS method ,the value is around -11.3dBm. So , the linearity has been improved by around 3dBm.The reasons for this increment is ,in conventional DS method only g3 is eliminated.Here 2 different MOSFET is available one has positive gs and another one has negative gs.So the overall g3 is almost zero as the cancel out each other.On the other hand, in modified DS method, both g2 and g3 is cancel out.Here g3 of both MOSFET are in such a phase that their total value is in the opposite direction of g2.And this way, g2 is cancel out and the linearity increases in modified DS method.

5.5.3 Noise Figure

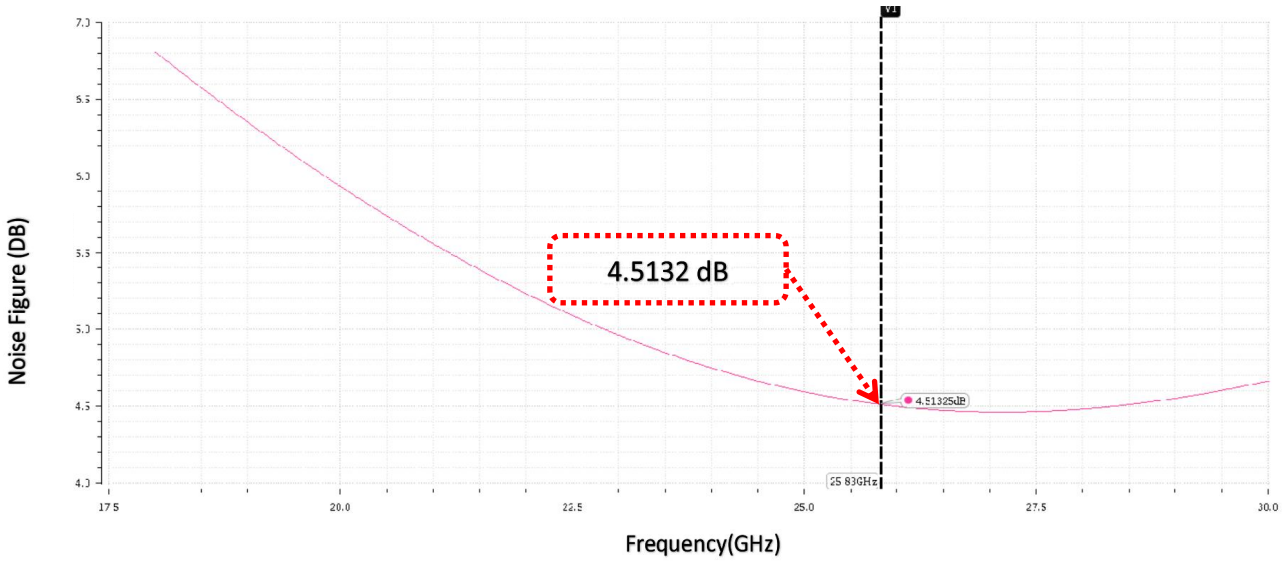

Fig 6.5.3 :NF curves for for 2 stage cascode with Modified DS in both stage and Post distortion

Here the Noise figure is around 4.5132dB in both stage modified DS and Post distortion technique.Here NF is still with in the reasonable range for 5G application.

6.6 Results

6.6.1 Data from the Proposed architecture

Table 6.6.1 : Data from the proposed architecture

Parameters	Value
Technology	Gpdk 90nm
Operating Frequency	25.83GHz
Froward Gain(S21)	13.154 db
Input Return Loss(S11)	-8.87 db
Output Return Loss(S22)	-4.04 db
Reverse Isolation	-39.82 db
Noise Figure	4.51
IIP3	-8.25
OIP3	5.1
Supply Voltage	1.2 volts
Power Consumption	20.21(mW)

Here , we can see the output of our proposed architecture.The operating frequency is 25.83GHz.The s parameters are -9.87dB,-39.82dB, 13,154dB,-4.04dB.The operating gain is 13.154 dB which is in the reasonable range for 5G application.The power consumption is also around 20.21mW which is also in the range because for 2 stage cascode the power consumption range is around 40mW.

6.6.2 Results for Different Techniques

Table 6.6.2: Results for Different Techniques

Topologies	2stage CS Cascode	2stage CS Cascode with DS	2stage CS Cascode with DS in both stages	2stage CS Cascode with DS in both stages and post distortion	2stage CS Cascode with modified DS in both stages and post distortion
Operating Frequency	25.83GHz	25.83GHz	25.83GHz	25.83GHz	25.83GHz
S11(db)	-24.0	−9.72975	−15.7881	−13.8316	-8.87
S12(db)	-37.067	−34.049	−31.865	−33.632	-39.82
S21(db)	18.254	16.945	14.447	12.676	13.154
S22(db)	-1.2827	−1.4786	-8.1742	−5.52	-4.04
IIP3	-19.1005	-17.5195	−14.3822	-11.3118	-8.28
Power Consumption(mW)	8.61	10.12	12.33	16.45	20.2158

Here ,we have provided the different parameter values based on different technique.In 2 stage cascode , the gain was quite high (around 18dB) which is gradually decreased in the futher techniques like 2stage CS cascode with DS, 2stage CS cascode with DS in both stage, 2stage CS cascode with DS in both stage and post distortion and 2stage CS cascode with modified DS in both stage and post distortion.On the other hand, the linearity has gradually increased from -19dBm to -8.28dBm.So overall ,the gain has decreased by 5dB where as the linearity has beed increased around 11dBm.As our main prority was to increased the linearity for high data rates uses.We think , we have achieved our desired result.

6.7 Comparison With the Other LNA from Different Papers

Table 6.7: Comparison With Other LNA from Different Papers

Specification	This work	[1]	[2]	[3]	[4]	[5]
Gain (dB)	13.154	17	18.5	27	25.6	18.1

NF (dB)	4.51	2.1-2.9	4.2-5.5	3.1-4.1	3.3-4.3	3.1
PDC (mW)	20.21(mW)	17.3	5.6	80	31.4	4
IIP3 (dBm)	-8.25	-14.4@ 22GHz	-9.4@ 28GHz	-12.5@ 32GHz	-12.6@ 27GHz	–6 @ 25.83GHz

The comparison between our work and other literature demonstrates key performance metrics essential for 5G applications. First, the gain achieved by your design is 13.154 dB. Although slightly lower than some other works, this gain is within the acceptable range of 10 dB to 20 dB for 5G applications, ensuring sufficient signal amplification.

Next, the noise figure (NF) of our work is comparable to other studies and falls within the 3 dB to 7 dB range required for 5G. This indicates that our design maintains a low level of noise, essential for clear signal transmission.

A significant advantage of our design is its power consumption. our work consumes considerably less power than other designs, staying well below the 40 mW threshold. This efficiency is crucial for practical applications, reducing operational costs and enhancing the overall sustainability of the technology.

Most notably, our design excels in achieving the highest Input Third-Order Intercept Point (IIP3) value among the compared works. A high IIP3 value is critical for ensuring linearity, which is the top priority in 5G applications to achieve high data rates. Linearity minimizes signal distortion, ensuring high-quality and reliable communication.

Overall, while our design's gain is slightly lower, its excellent noise figure, low power consumption, and superior IIP3 value make it highly competitive and suitable for 5G applications. These attributes collectively demonstrate the robustness and efficiency of our design in meeting the stringent demands of modern communication systems.

Chapter 7

Conclusion

7.1 Summary

This works represents a 90nm, highly linear, low noise, high power-gain, CMOS am-plifier in the millimetre wave band for 5G applications. The amplifier is linearized using three different methods in the suggested topology.The common source stage mosfet-induced nonlinearity in the cascode structure is suppressed by the robust derivative superposition technique. This non-linearity is further eliminated by adding three post-linearization branches. These post-linearization branches improve linearity and maximize power usage. Furthermore, a parallel-connected folded cascade pmos reduces the non-linearity generated by the cascode structure's shared gate stage mosfet. Simulations show that at an operating frequency of 25.83GHz, which covers the mm wave band, the circuit achieves a gain of 13.154dB and a noise figure of 4.51dB while consuming 20.21mW of power. The design has exceptional linearity performance using the several linearity techniques for a cascode structure, yielding a positive IIP3 of -8.25 dbm.

7.2 Scope For Future Work

7.2.1 Minimization of Power Consumption

Table 5.6.1 shows that a 1.2-volt source must provide 20.21 milliwatts of power for the architecture that is being shown. This is a comparatively high power requirement for amplifiers with minimal noise. The excessive number of extra mosfets utilised to increase linearity is the cause of this high power usage. These mosfets utilise a significant amount of power even though their widths are smaller than the main amplifier's. As a result, additional element optimisation is possible to lower the energy use. But while doing so, one should be aware that there will be additional costs, including a reduction in power gain.

7.2.2 Reduction od Number of Mosfets

The suggested architecture improves linearity by combining three distinct methods. This means that a lot of mosfets are needed. These mosfets have a number of drawbacks. They start by making the circuit use more power. Furthermore, they take up important chip space, which raises the price. Reducing the number of transistors in the design will result in lower fabrication costs, lower power consumption, and the ability to operate the circuit at a lower biassing voltage.

7.2.3 Improvement of 3 dB compression Point

An LNA's linearity is shown by a metric called the 3 dB compression point. This is the signal's input power level, which results in a 3dB decrease in gain from its interpolated extended value. A low 3dB compression point may be able to restrict the circuit's dynamic range. Our suggested architecture has a comparatively low 3dBCP of -8.28 dBm. This indicates that a wider range of input power levels cannot be handled by our amplifier without distortion due to its restricted dynamic range. By including derivative superposition branches that selectively consume the circuit's third-order current and post-linearization circuits, our suggested architecture improves the circuit's linearity.

7.2.4 Physical Implications

The results displayed were obtained solely through simulation. The behavior of fab- ricated ICs may differ from the simulation results. Consequently, the circuit must be designed for fabrication, and the performance of the fabricated IC can then be com- pared to the simulation results. In our architecture, the analog capacitors and inductors are MIM (Metal-Insulator-metal) capacitors and two coupled spiral octagonal inductors, which are actually employed in the fabrication of ICs. The layout design of the circuit, static timing analysis, transmission delay modeling, parasitic extraction, placement, and routing are included in the design procedure of the circuit for fabrication.

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